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Standalone Operation of Modified Seven-Level Packed U-Cell Inverter for Solar Photovoltaic System

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ABSTRACT

In this paper, a modified configuration of Single-Phase Seven-Level Packed U-Cell (PUC) Multilevel Inverter for solar photovoltaic system is presented & investigated for standalone operation. The Seven-Level MPUC Inverter comprises of six semiconductor switches & two DC links which generates seven voltage levels at the inverter output. The maximum amplitude of inverter output voltage is more than that of available maximum DC link value (i.e. sum of two DC link values). The voltage levels generated in the MPUC inverter is more with reduced number of components counts as compare to conventional multilevel inverter topologies like Cascaded H-Bridge (CHB) and Neutral Point Clamped (NPC). The proposed inverter finds application in PV System where green power is derived from two PV panels with different power rating and voltage rating connected to DC links. Several design considerations viz. the RMS value of inverter output voltage, switching frequency & voltage rating of semiconductor switches are taken into consideration to prove the advantages of the MPUC inverter. The simulation results of the MPUC inverter shows the appropriate operation of multilevel inverter.

1. Introduction

Owing to growing number of consumers in addition to large scale power industries, the power grid has experienced large energy demand from last decade. Traditional bulky transformers are significantly replaced by power electronic devices because a lot of research work is happening in power electronic field these days resulting in advancement of semiconductor device technology. Power converters are utilized as a conversion medium for transferring green power either for grid or a standalone load. Economic pricing of power semiconductor devices makes it beneficial to produce and allow them in competitive market. Recently, the use of a greater number of switches in the converter causes no significant rise in pricing. This is the reason that the traditional two-level converters having high harmonics and power losses are being interchanged by the multilevel inverters having less switching frequency [1, 2].

Now, the focus of researchers has moved towards developing various topologies of multilevel inverters and their control strategies. So, the foremost attention is to reduce the component counts in these inverters. Fewer the component counts, lower the cost and power loss [3]-[5]. The two most popular commercially available multilevel inverter (MLI) topologies are CHB and NPC inverter topologies [6].

Recently, the flooding of green power into the grid has become a prime concern [7]. Most of the countries have initiated to implement the solar power panels at broad scale to cater the local energy need. With the use of power electronic converters, the DC power is converted into AC power which is further transferred to the grid or a standalone load.

Thus, the improvement in conversion efficiency and reduction in power loss of these converters are tackled in several reports [8-9]. Conversion of DC voltage of PV system into AC waveform with low harmonics to be used by the grid or standalone load with high conversion efficiency and small size filtering requirement can be fulfilled by single-phase multilevel inverters (MLI) [10].

The key problem with most of the topologies are to use numerous isolated DC sources which makes it difficult for its practical implementation. An isolated DC source can be made by an AC transformer and diode bridge rectifier which is a costly affair and become bulky for manufacturing. Consequently, topologies having single DC source i.e. NPC (Neutral Point

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Clamped) inverter and five-level PUC (PUC5) inverter [11] are commercially more viable than other new topologies. Nevertheless, some topologies e.g. CHB are utilized for very high-power applications owing to necessity of large number of DC sources.

In latest survey, seven-level PUC inverter topology was introduced which has many advantages like low component counts and numerous output voltage levels [12]. The key problem with PUC inverter is its maximum output voltage level which is actually the maximum available DC link value of the topology. In recent times, a seven-level modified PUC inverter topology has been presented which provides an alternative for those applications where several Photovoltaic panels are available for connecting it to isolated DC links. In [13], the authors demonstrated that Photovoltaic panels having different voltage rating & power rating can be coupled with two DC link of modified PUC inverter topology.

In this paper, modification of Seven Level Packed U-Cell inverter is done for solar PV systems. MPUC inverter topology is similar to CHB inverter having unequal DC sources where two cells produces seven voltage levels. The introduced inverter has a smaller number of semiconductor switches than the CHB inverter with equivalent performance. In MPUC inverter, two unequal DC sources (i.e. two PV panels with different power rating) are required to generate seven output voltage levels by means of reduced harmonic and uniformly distributed voltage levels. The maximum inverter output voltage level is sum of amplitudes of two dc sources. So, authors call it as Modified PUC Inverter (MPUC).

The seven-level PUC inverter is elaborated in section II. Subsequently, seven-level MPUC topology is described in section III. The rms value of seven level inverter output voltage for standalone operation is discussed in section IV. The results obtained from simulation of MPUC inverter has been given in section V. Conclusion is specified under section VI.

2. Seven-Level Packed U-Cell Inverter

The template is used to PUC inverter topology was first introduced by Al-Haddad in 2010 & later it was advanced by Hani Vahedi in 2015 [14]. PUC inverter is among the most promising multilevel inverters which takes advantages of both Flying Capacitor Converter (FCC) & CHB inverter. This topology is known as Packed U-Cell as the shape of each inverter unit is in U form. In Each U Cell, it contains two semiconductor switches & one DC voltage source. PUC topology work only with one DC source & a smaller number of active and passive components. Six semiconductor switches with anti-parallel diodes are used to achieve seven voltage levels which is evident from figure 1.

These 6 switches are divided into two legs having three switches in each leg. In one leg, there are three main switches (Q_1, Q_2 & Q_3) and in another leg, there are three complimentary switches of main switch ($Q_{1'}$, $Q_{2'}$ & $Q_{3'}$).

Various voltage levels are achieved either through DC voltage sources available or through their series opposition provided the amplitude of second DC source (V_2) is equal to one third of amplitude of first DC voltage source (V_1) i.e. $V_1 = 3V_2$. Thus, inverter output voltage has seven-voltage levels i.e. 0, $\pm V_2$, $\pm 2V_2$, and $\pm 3V_2$. From the Table I, it can be concluded that there are 3 positive voltage levels, 3 negative voltage levels and 2 zero voltage levels (viz. state 4 and 5). All eight switching states are shown graphically in Figure 2. Zero voltage level can be achieved only when the load is either shorted through main switches or through complimentary switches. Redundant zero voltage states are utilized by appropriate means just for reduction in switching frequency at the time when there are changeover in between positive & negative half cycles of AC signal.

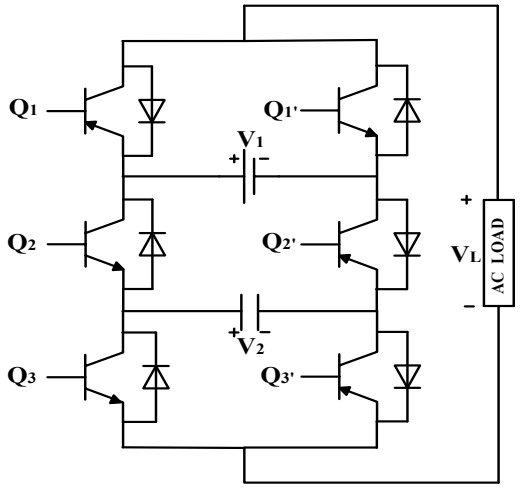

Figure 1: Packed U-Cell (PUC) Inverter Topology

Table 1: Complete Switching States & Voltage Levels

Switching States	Q_1	Q_2	Q_3	$Q_{1'}$	$Q_{2'}$	$Q_{3'}$	$V_{inv} = V_L$
1	1	0	0	0	1	1	V_1
2	1	0	1	0	1	0	$V_1 - V_2$
3	1	1	0	0	0	1	V_2
4	1	1	1	0	0	0	0
5	0	0	0	1	1	1	0
6	0	0	1	1	1	0	$-V_2$
7	0	1	0	1	0	1	$V_2 - V_1$
8	0	1	1	1	0	0	$-V_1$

From above switching states Table I, it can be concluded that irrespective of change in switching frequency and carrier frequency of adopted PWM technique, the switches Q2 & Q2' operate at line frequency (i.e. 50 Hz). This results in significant reduction of switching losses. Thus, the switches produce flow of current in the DC bus resulting in the use of a series diode for blocking the reverse voltage. To overcome this problem, an energy storage element i.e. Capacitor is used as a second DC source. The voltage across capacitor must be one third to that of V1 which can be achieved by various voltage balancing techniques. The current through the capacitor is in positive and negative parts which shows that there is charging and discharging in the capacitor [15]-[19]. Thereby achieving the desired voltage level for generating constant desired inverter output level. The biggest issue in using PUC inverter topology is its low maximum voltage level i.e. the maximum amplitude of the PUC inverter topology is maximum value of amplitude of the two voltage sources. Thus, the PUC inverter can't generate voltage more than the maximum value of the two voltage sources. So, it doesn't get application in medium or high-power applications [20]-[23].

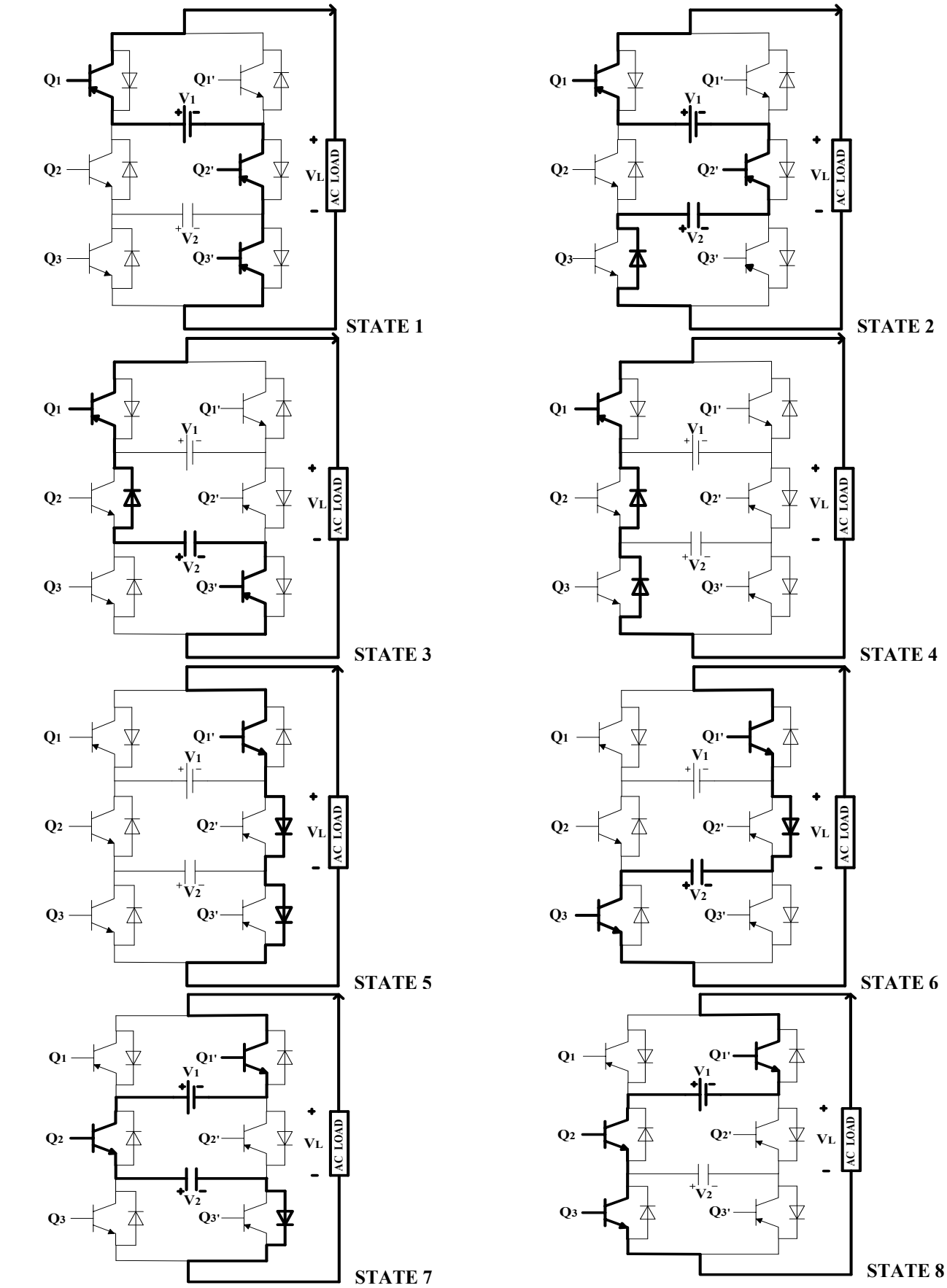

Figure 2: Switching States for PUC Inverter Topology

3. Seven-Level Modified Packed U-Cell Inverter

Due to recent advancement in solar panels and its economic cost, it becomes feasible to use number of PV panels as DC sources. Hence multilevel inverters using large number of DC sources are justified economically. The maximum output voltage in PUC inverter is not more than that of maximum DC voltage source magnitude. To solve this issue, the MPUC inverter topology is proposed as shown in figure 3. The DC source (V_2) is attached in reverse direction when compared to PUC inverter. So, the lower switches viz. Q_3 & $Q_{3'}$ have also been reversed to hinder current through diodes. Thus, with appropriate use of gate pulses, the path of current flow can be allowed or hindered. Various Switching states & output voltage levels for MPUC inverter is shown in Table II. From table II, it can be concluded that maximum inverter output voltage of MPUC inverter is nothing but total addition of two DC voltage sources i.e. V_1+V_2 which can be obtained by joining two voltage sources in series. Thus, we are getting more voltage amplitude by this proposed topology. It is evident that seven uniform voltage level is produced by MPUC inverter provided the second DC source (V_2) amplitude is two times the first DC source (V_1) amplitude i.e. $V_2 = 2V_1$. So, the output voltage levels have following levels: 0, $\pm V_1$, $\pm 2V_1$, $\pm 3V_1$. Thus, the maximum output voltage amplitude will be $3V_1$ while maximum DC source is equal to $2V_1$. The voltage level $3V_1$ is obtained by joining two DC voltage source V_1 & V_2 in series which appear on load. The voltage level $2V_1$ can be achieved by making second DC voltage source V_2 to be appear on the load. The voltage level V_1 can be achieved by making first voltage source V_1 to be appear on the load [24]-[26].

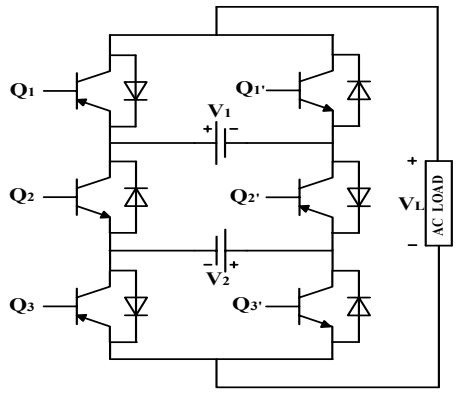

Figure 3: MPUC Inverter Topology

Table 2: Complete Switching States & Voltage Levels

Switching States	Q_1	Q_2	Q_3	$Q_{1'}$	$Q_{2'}$	$Q_{3'}$	$V_{inv} = V_L$
1	1	0	0	0	1	1	$V_1 + V_2$
2	1	0	1	0	1	0	V_2
3	1	1	0	0	0	1	V_1
4	1	1	1	0	0	0	0
5	0	0	0	1	1	1	0
6	0	0	1	1	1	0	$- V_1$
7	0	1	0	1	0	1	$- V_2$
8	0	1	1	1	0	0	$- V_1 - V_2$

Eight switching states are presented graphically in figure 4. Here are two redundant zero voltage states viz. state 4 and 5 which is used in the reduction of switching frequency. When zero voltage level is required to be generated at the output, the modulation technique selects the appropriate state in state 4 and 5 to give gate pulse to switches which gives less change in Turn-On & Turn-Off mode of operation resulting in significant reduction in switching frequency. From the switch states shown in table II, it can be concluded very clearly that irrespective of change in switching & carrier frequency, the two switches viz. Q_2 & $Q_{2'}$ operate at the line frequency i.e. 50 Hz.

4. Design Consideration of Standalone Operation

A mathematical analysis has been done for the standalone application of MPUC inverter supplying power to single-phase load. Here we aim to determine general expression for output voltage waveform of seven-level MPUC inverter based on figure 5.

The general expression for determining RMS voltage is given by:

$$V_r = \sqrt{\frac{1}{T}\int_0^T v_0^{\,2}(t)\,dt} \tag{1}$$

where Vr is RMS voltage, v_0 is time function of voltage and T is time period of the periodic function.

Thus equation (1) can be rewritten as follows:

$$V_r = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} v_0^{\,2}(t)\,dt}$$

$$= \sqrt{\frac{1}{2\pi}\left[4\int_{\theta_1}^{\theta_2} V_1^{\,2}\,d\omega t + 4\int_{\theta_2}^{\theta_3} V_2^{\,2}\,d\omega t + 2\int_{\theta_3}^{\theta_4}\left(V_1+V_2\right)^2 d\omega t\right]}$$

$$= \sqrt{\frac{1}{2\pi}\left[4V_1^{\,2}\alpha + 4V_2^{\,2}\beta + 2\left(V_1+V_2\right)^2\gamma\right]} \tag{2}$$

Since $V_2 = 2V_1$

$$V_r = \sqrt{\frac{1}{2\pi}\left[4V_1^{\,2}\alpha + 4\left(2V_1\right)^2\beta + 2\left(3V_1\right)^2\gamma\right]}$$

$$= V_1\sqrt{\frac{2\alpha + 8\beta + 9\gamma}{\pi}} \tag{3}$$

where α , β and γ are angles at which reference signal crosses voltage levels as fixed lines between the carriers. The RMS value of output voltage can also be determined in term of modulation index (m_a) and maximum output voltage level ($V_{max} = 2V_1$) which is given as follows:

$$V_r = 0.725 \times m_a \times V_{max} \tag{4}$$

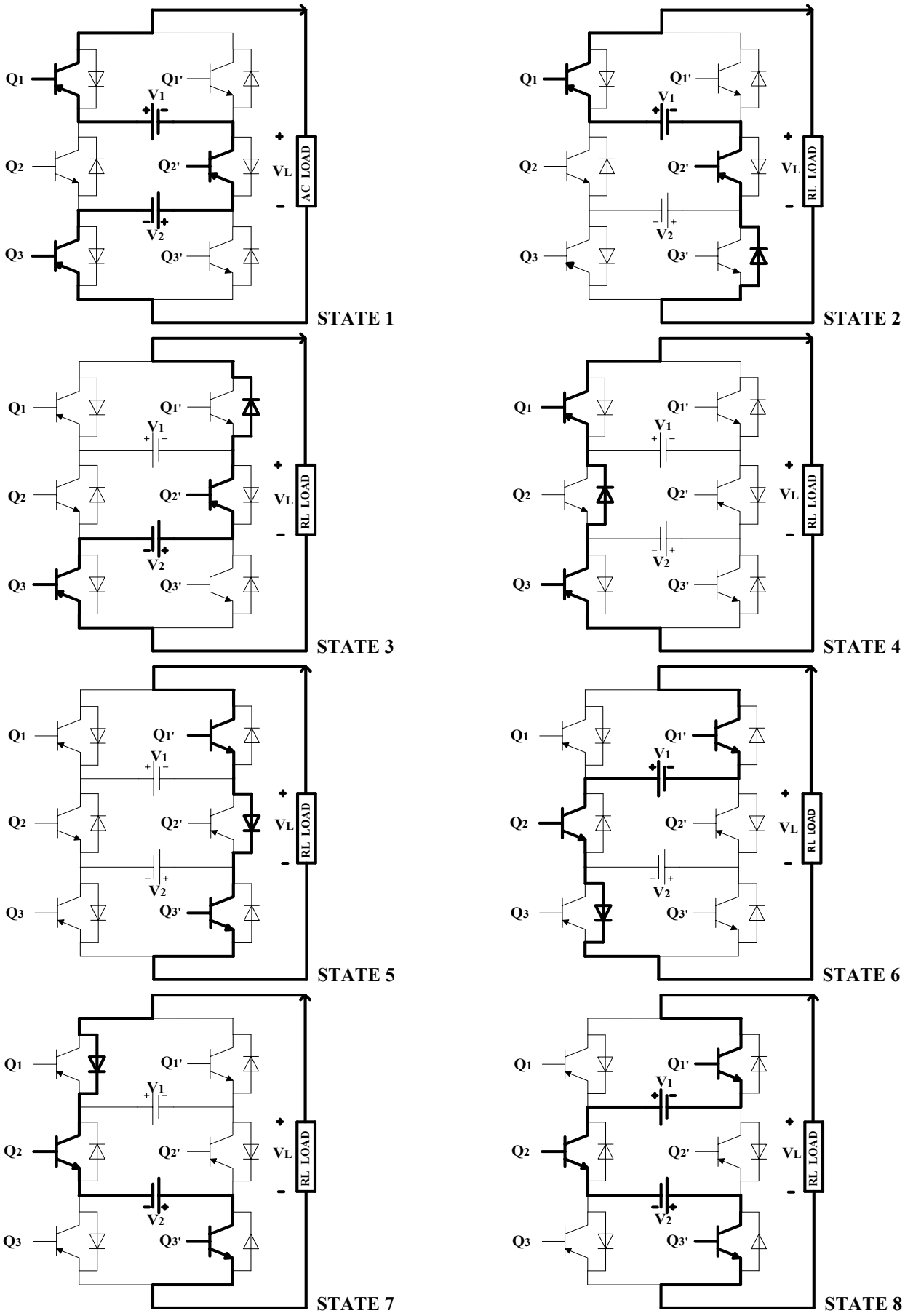

Figure 4. Switching States for MPUC Inverter

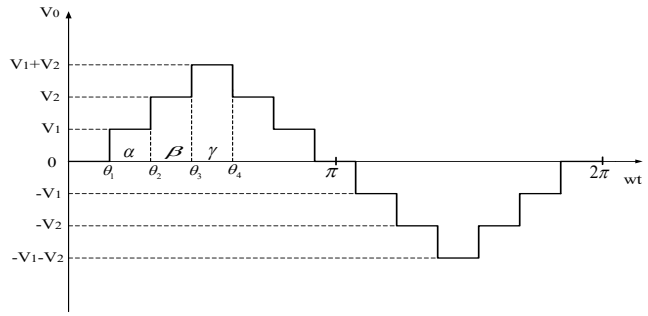

Figure 5: Seven-Level Inverter Output Voltage Waveform

5. Simulation & Results

The introduced MPUC inverter topology is simulated in standalone mode of operation to validate the above analysis. Six IGBT switches are taken in the simulation model. The switching algorithm adopted is elucidated in [16] where four level shifted carriers are used for modulating the reference signal. Thus, gate pulses are given to all the six pulses. Table III gives complete view of simulation parameters.

Here two DC sources viz. V_1 and V_2 are joined to different DC links of PV panels having different power & voltage rating and standalone load has been taken at the output. At higher switching frequency, passive components size reduces significantly.

Here the MPUC inverter is connected to RL load because most of the AC loads are inductive in nature. The parameters of RL load is specified into table III and results obtained from simulation has been given in figure 6.

The inverter output voltage waveform i.e. V_{inv} has seven uniform voltage levels having maximum of 120 Volt i.e. the total addition of two DC sources. The uniformly distributed & symmetric structure of inverter output voltage & current shows proper selection of modulation technique. THD of inverter output voltage waveform with no use of any filter is 23.96 % which is evident from figure 7. THD for output current waveform is 1.24 % which is evident from figure 8. Thus, the current THD is less than 5 % which is as per IEEE STD 519. Thus, the filtering requirement will be small and economical for MPUC inverter applications especially renewable energy.

For determining switching frequency of MPUC inverter topology, the inverter output voltage as well as gate pulses for switches Q_1, Q_2 & Q_3 has been shown for one time period of output voltage which is given in figure 9. Based on number of switching pulses for one cycle, we can determine the switching frequency of MPUC inverter switches which is given in table IV. Since each switch in one U cell operate in complimentary, so both the switches in a U cell will have same frequency. During switching time, the upper switches viz. Q_1 & Q_1, have to block voltage V_1 & lower switches viz. Q_3 & Q_3, have to block voltage V_2. So, the voltage rating of upper switches and lower switches are V_1 and V_2, respectively. The two middle switches viz. Q_2 & Q_2, have to suffer higher voltage than other switches i.e. V_1+V_2. So, the voltage rating of two middle switches are V_1+V_2.

The middle switches operate online frequency i.e. 50 Hz. So middle switches operating online frequency and high power are placed into middle U cell. Thus, a comparative study based on component counts is performed among popular Cascaded H-Bridge (CHB) inverter & MPUC inverter. The main limitation of MPUC inverter is that the unequal shading of Photovoltaic panels may cause deterioration of power balance between two DC links which may lose voltage control.

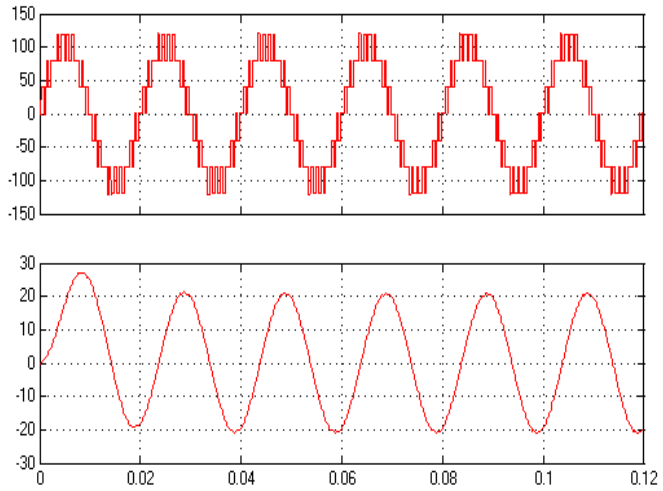

Figure 6: MPUC Inverter Output Voltage & Current Waveform

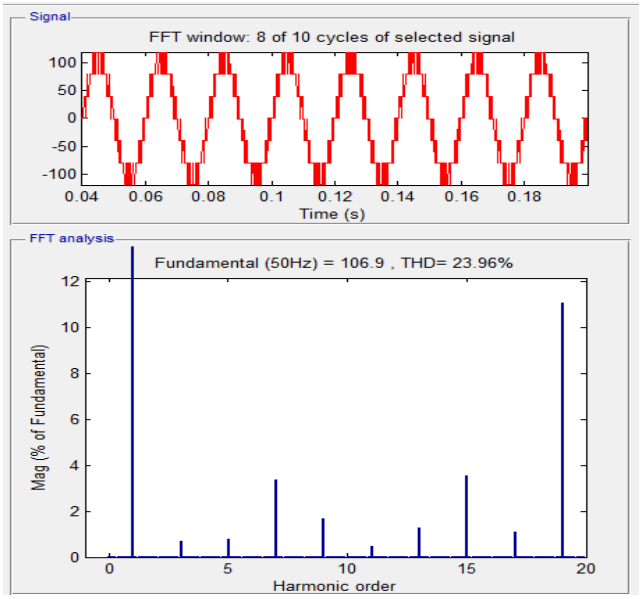

Figure 7: FFT Analysis for Inverter Output Voltage

Table 3: Parameters Used in Simulation

Parameters	Values
First DC Source (V_1)	40 Volt
Second DC Source (V_2)	80 Volt
Frequency (f)	50 Hz
Switching Frequency (f_{PWM})	1 KHz
Resistance (R)	2 ohm
Inductance (L)	15 mH

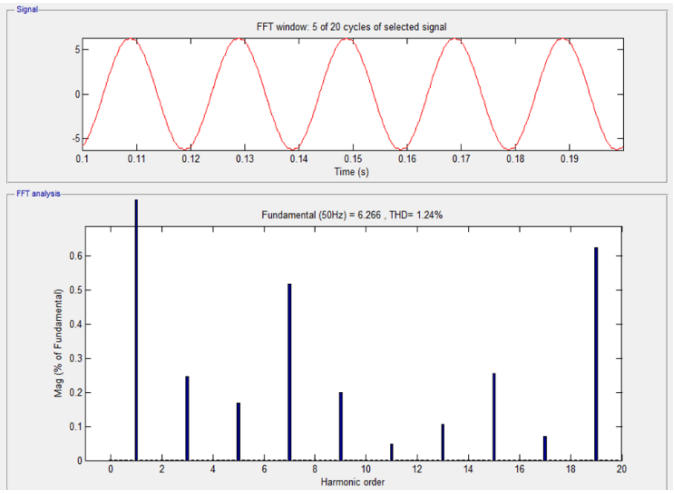

Figure 8: FFT Analysis for Inverter Output Current

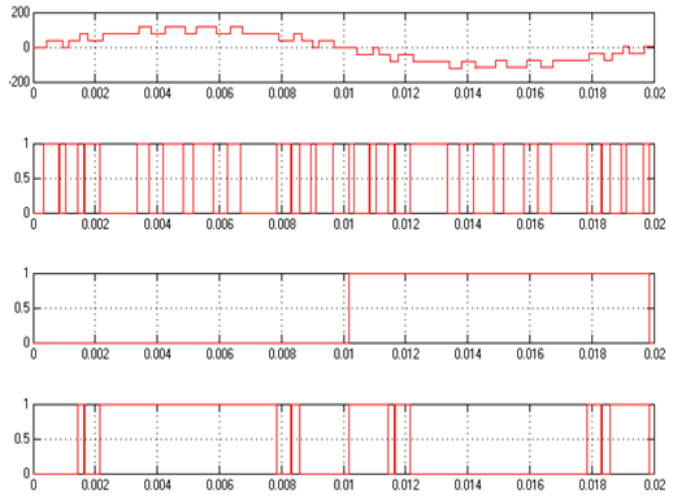

Figure 9: One Complete Cycle of (i) Inverter Output Voltage (ii) Q_1 Gate Pulse (iii) Q_2 Gate Pulse (iv) Q_3 Gate Pulse

Table 4: Switching Frequency of Inverter Switches

Q_1 & Q_1'	1250 Hz
Q_2 & Q_2'	50 Hz
Q_3 & Q_3'	500 Hz

Table 5: Comparative Study of Component Counts

Topology	Number of Switches	DC Sources
7-level CHB (Equal DC Sources)	12	3
7-level CHB (Unequal DC Sources)	8	2
7-level MPUC Inverter	6	2

6. Conclusion

In this paper, the modified form of Packed U-Cell inverter topology has been presented and validated on MATLAB Simulink. The proposed MPUC topology can generate seven levels of inverter output voltage with acceptable harmonic contents. Unlike PUC topology, the proposed topology is capable to produce maximum output voltage level which is more than the available maximum voltage source. In this topology, the DC source amplitudes gets added so that it can supply more power at the output. The switching algorithm adopted in MPUC inverter is such that it can operate at less switching frequency. Furthermore, this topology is targeted for PV applications for delivering power from different voltage rating PV panels. To show this, simulation results are given to verify THD for inverter output voltage & output current. Likewise, the comparison of MPUC inverter & CHB inverter proved the suitability of proposed inverter for advantages like fewer component counts, economical manufacturing cost and compact package owing to reduced filter size.

Conflict of Interest

The authors declare no conflict of interest.

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