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# On The Development of a Reliable Gate Stack for Future Technology Nodes Based on III-V Materials

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ABSTRACT

*In this work, we discuss how the insertion of a $LaSiO_x$ layer in between an in-house IL passivation layer and the high-k has moved the III-V gate stack into the target window for future technology nodes. The insertion of this $LaSiO_x$ layer in the gate stack has reduced the $D_{it}$ and $N_{bt}$ below the target level of $5x10^{11}$ /eV.cm$^2$ and $3x10^{10}$ /cm$^2$ (target at 10 years operation: $\Delta V_{fb}$<30mV at 125°C) respectively. From physical analysis, it was found that $LaSiO_x$ can stabilize the interaction of the IL layer with the InGaAs substrate. An implant free $In_{0.53}Ga_{0.47}As$ n-MOSFET was fabricated with this gate stack and for the first time, a III-V gate stack meets the reliability target for advanced technology nodes with a max operating $V_{ov}$ of 0.6 V. In addition, an excellent electron mobility ($\mu_{eff,peak}$=3531 cm$^2$/V-s), low $SS_{lin}$=71 mV/dec and an EOT of 1.15 nm were obtained. We also report the scaling potential of this stack to 1 nm EOT without any loss in performance, reliability and further reduction of the sub-threshold swing ($SS_{lin}$=68 mV/dec).*

## 1. Introduction

III-V compound semiconductors have already been widely investigated as an alternative material to Silicon for future Metal - Oxide-Semiconductor Field Effect Transistors (MOS-FETs). MOS devices based on III-V compound semiconductor materials like InGaAs, with excellent performance, have been demonstrated on both 2-inch InP substrates and on a 300mm Si platform [1-5]. But, in order to become a commercially viable alternative to existing Si technologies, two major issues are yet to be solved: 1) the defective interface between III-V materials and the high-k oxide layers, and 2) the high density of defects in the most commonly investigated high-k oxides, $Al_2O_3$ and $HfO_2$.

Both of these issues have been shown to affect almost every aspect of device performance, such as the capacitance [6-11], reliability of III-V based devices [11-14], on-state electrical parameters like mobility [15], and trans-conductance [16, 17]. As a result, it becomes extremely important to reduce their impact in order to make commercial III-V MOSFET technology a reality. In this regard, the use of a new IL layer in combination with an $Al_2O_3/HfO_2$ or just $HfO_2$ stack was reported, showing improved performance and a significant reduction of the oxide traps. However, with the requirement of a thin $Al_2O_3$ layer for gate stack thermal stability and due to the wide defect distribution in $Al_2O_3$, the total density of charging oxide traps was still higher than the target (10 years reliability target: flat-band voltage shift, $\Delta V_{fb} < 30$ mV at 125°C. Assuming a typical time power law exponent of 0.13, the failure criterion projects effective density of charged defects, $\Delta N_{eff}$ to < $3x10^{10}$/cm$^2$ at operating field, for an Effective Oxide Thickness (EOT) of 1 nm [18, 19]).

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This paper is an extension of the work presented in *IEEE Symposium on VLSI Technology 2017*. In this paper, we demonstrate and comprehensively discuss on the process of replacing $Al_2O_3$ in the IL/$Al_2O_3$/$HfO_2$ gate stack with $LaSiO_x$. Furthermore, we elaborate on the improvements, thereof, in the interface properties and reliability for operation at $V_{DD}$=0.8 V, which exceeds the operating target for future technology nodes without any loss in the electrical performance of the MOSFET device reported earlier.

## 2. Experimental details

Capacitors were made starting from an MBE grown 300 nm n-type $In_{0.53}Ga_{0.47}As$ on 2-inch n-type InP substrates. The targeted Si doping in the $In_{0.53}Ga_{0.47}As$ grown layer was ~$1x10^{17}$ at/$cm^3$. Prior to the gate stack deposition, the substrates were cleaned in a 2M HCl solution for 5 min at room temperature and subsequently rinsed in de-ionized water. $H_2S$ pretreatment and deposition of the IL (Inter Layer), $LaSiO_x$, $Al_2O_3$ and $HfO_2$ were done in an ASM Pulsar® 3000 ALD reactor. The $H_2S$ pretreatment is done in-situ prior to the high-κ deposition. The IL used here is an ALD based layer with a κ-value ~6. The $H_2S$ treatment and IL film deposition are both done at 250°C. $Al_2O_3$ and $HfO_2$ were deposited by ALD TMA/$H_2O$ and $HfCl_4$/$H_2O$ at 300°C. $LaSiO_x$ is deposited by an ALD process at 250°C using the following precursors: LoLaPrime® (AIR Liquide), $SiCl_4$, $H_2O$. A 42% La concentration in the $LaSiO_x$ is obtained by using a La:Si pulse ratio of 1:5. A full ALD cycle consists of : [[$SiCl_4$/purge/H2O/purge] x 5 + [LolaPrime/purge/$H_2O$/purge] x 1] x n. Under these conditions, a GPC of 0.1754 nm is achieved.

Dot capacitors were fabricated by sputtering 80 nm TiN using physical vapor deposition (PVD). A dry-etch process was used to etch the metal gate. An anneal in forming gas (10% $H_2$/$N_2$) was done prior to metal deposition (PDA) or post metal deposition (PMA) at 400°C for 5 min.

Implant-free quantum-well devices were also fabricated to study the impact of these passivation schemes on the device performance and reliability. A schematic diagram of the quantum-well MOSFET is shown in Fig.1. The stack for MOSFETs consists of a 15 nm un-intentionally doped $In_{0.53}Ga_{0.47}As$ channel layer, a 3 nm InP etch stop layer and a 50 nm n+ $In_{0.53}Ga_{0.47}As$ (Si-doped, $1x10^{19}$ $cm^{-3}$) layer, all grown on a 2-inch semi-insulating InP substrate. Fig. 2 describes the process flow used in this work. The detailed device fabrication can be found in [20]. Prior to gate stack deposition, a digital etch (cycles of HCl and $H_2O_2$) was used to clean and smoothen the InGaAs channel surface. The different gate stacks that were studied are depicted in Table I.

I-V and C-V measurements were used to study the impact of the gate stack on the performance of the devices. I-V measurements were carried out using HP4156 parameter analyzer and C-V measurements were performed using a HP4284A-LCR meter. The interface defect density, $D_{it}$, is extracted using the conductance method from the parallel equivalent conductance $G_p$ [21] at room temperature. The amount of oxide traps ($\Delta N_{eff}$) are measured by C-V hysteresis measurements (forward and reverse sweep of the gate voltage) at different maximum stress voltages and the corresponding shift in flat band voltage, $\Delta V_{fb}$, measured between the forward and backward trace is converted into a sheet charge ($\Delta N_{eff}$ ($E_{ox}$)). The flat-band voltage is the gate voltage corresponding to an inflection point in the double derivative of the normalized capacitance-voltage data at a frequency of 100 kHz [21,22]. The $\Delta N_{eff}$ at target field as well as the voltage acceleration

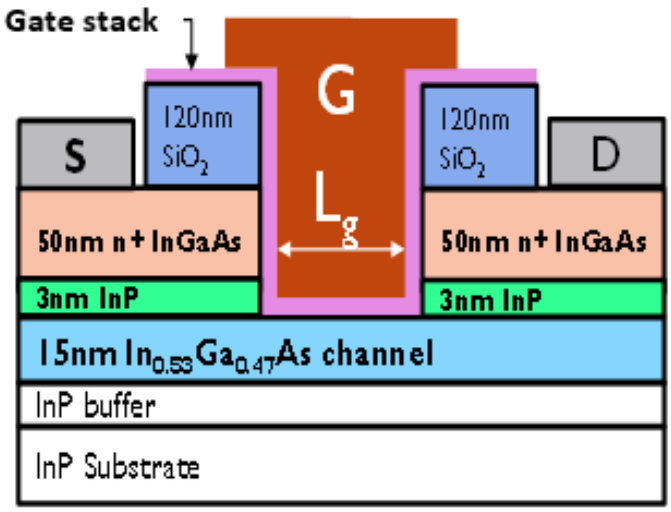


Figure. 1. Schematic representation of the MOSFET device (Dimensions are not to scale).

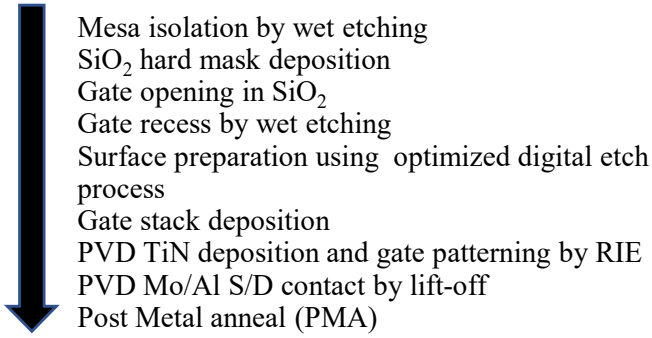


Figure 2. Process flow used in this work for MOSFET fabrication.

Table 1: Split table of III-V gate stacks

| Sample ID | Dielectric |
|---|---|
| Ref | 3 nm $HfO_2$ |
| A | 1 nm IL/3 nm $HfO_2$ |
| A' | 0.5 nm IL/3 nm $HfO_2$ |
| B | 1 nm IL/1 nm $Al_2O_3$/3 nm $HfO_2$ |
| B' | 1 nm IL/0.2 nm $Al_2O_3$/3 nm $HfO_2$ |
| C | 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ |
| C' | 1 nm $LaSiO_x$/3 nm $HfO_2$ |

factor (γ, i.e. the slope of the log-log plot of $\Delta N_{eff}$ vs $E_{ox}$) is reported as a figure of merit to study the oxide trap behavior [23]. Although this method does not take into account the influence of stress temperature and stress time into account, it helps in identifying the trends between different gate stack/pretreatments. Bias temperature instability (BTI) characterization using extended Measure-Stress-Measure (eMSM) technique was used to evaluate the reliability of the MOSFET devices [23]. Finally, Time-Of-Flight Secondary Ion Mass Spectrometry (TOFSIMS) was used to study the chemistry of the stacks.

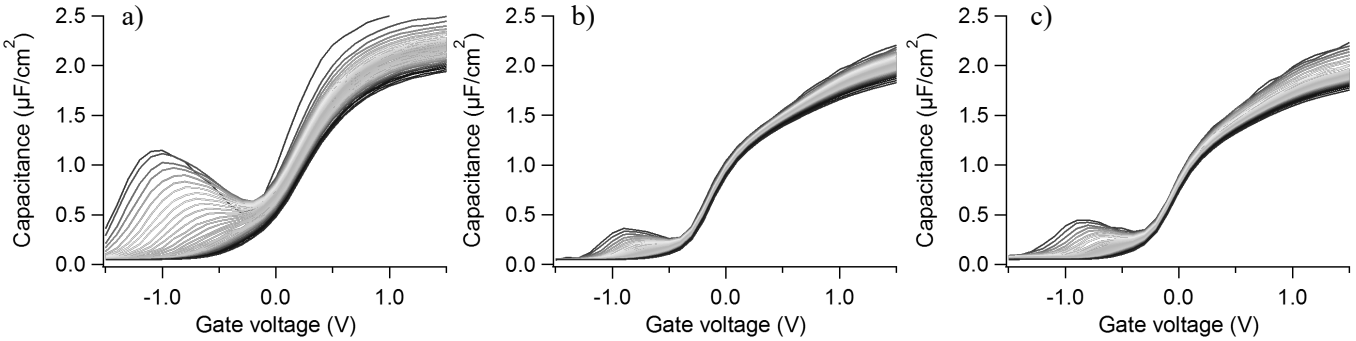


Figure 3. Measured RT CV's of gate stacks a) 'ref', b) A and c) B' described in Table I at 31 frequencies between 1kHz and 1MHz. The MOSCAP devices received a PDA at 400°C, 5' in Forming gas.

## 3. Results and discussion

### *3.1. The IL layer development and thermal stability*

Fig. 3 shows the multi-frequency (1 kHz - 1 MHz) C-V for various samples in the split table of Table I, measured at room temperature. The reduction in the $D_{it}$ bump and in frequency dispersion when inserting the IL (3-A,B') between the InGaAs channel and the $HfO_2$ layer clearly shows the improvement. Fig. 4 shows the result of the extraction of various electrical parameters from the measured C-V data. The extracted mid-gap $D_{it}$ drops by more than a factor of 2 when inserting the IL accompanied with a negative flat band voltage, $V_{fb}$, shift (Fig. 4a,b). An $H_2S$ treatment prior to the $HfO_2$ deposition has a similar effect: it reduces the $D_{it}$ and shifts the $V_{fb}$ by -0.15 V. Compared to an $H_2S$ treatment, the insertion of 1 nm of the IL layer shifts the $V_{fb}$ to even more negative values and a larger reduction in $D_{it}$ is observed. In addition, the IL layer reduces the $\Delta N_{eff}$ by 1 order of magnitude and increases the γ-value to 2.5. Although 0.5 nm of the IL layer shows similar trends, an optimum is reached when using 1nm of the IL layer. This result suggests that 1 nm of IL is needed to form a closed layer passivating the interface. When adding a thin (0.2 nm) $Al_2O_3$ cap on top of the IL layer, the $D_{it}$ bump and frequency dispersion increase slightly (Fig. 3-B'). One can also observe that the $V_{fb}$ shifts to more positive values and this goes hand in hand with a slight increase in $\Delta N_{eff}$ and reduction of the γ value. From these observations, a hypothesis can be put forward. Fig. 5 depicts

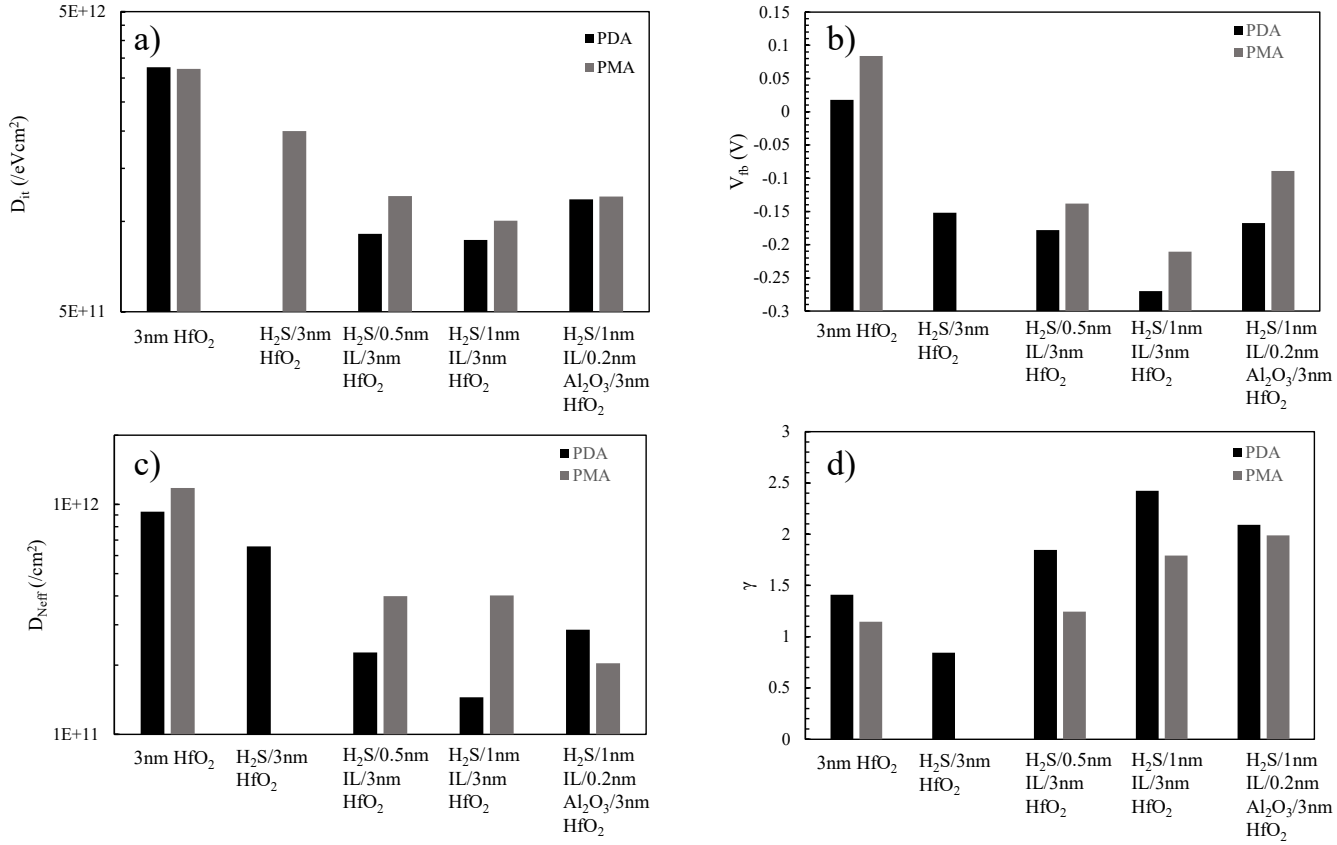


Figure 4. Electrical parameters extracted for gate stacks 'ref', A, A', B' described in Table I. a) Midgap $D_{it}$ extracted from RT CV's. b) $V_{fb}$ c) $\Delta N_{eff}$ extracted from RT CV hysteresis by converting the measured $\Delta V_{fb}$ into an effective charge sheet at the interface by: $\Delta N_{eff}=\Delta V_{fb}*C_{ox}/q$, and reported at charging equivalent field of 3.5 MV/cm [13]. $V_{start}$ condition was taken at $V_g$=-1.5V. d) Field acceleration exponent, γ, i.e. the slope of the log-log plot $\Delta N_{eff}$ vs oxide field which is a measure of the misalignment between the channel carrier energy-i.e. InGaAs $E_f$- and defect levels in the high-*k*. Filled bars represent the data after PDA, shaded bars represent the data after PMA.

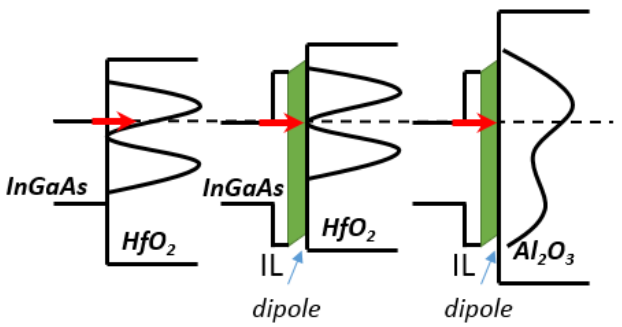


Figure 5. Defect band model to explain the observed changes in the γ value and total amount of charged oxide traps at a given field. The IL passivation layer is creating a dipole shifting the misalignment between InGaAs $E_f$ and defect levels in the high-κ. In $Al_2O_3$ a partial overlap between deep and shallow traps is existing [9] and an almost uniform defect band is present. Therefore, the dipole created is not as effective as compared to the situation where deep and shallow traps are well separated as is proposed for the stack with $HfO_2$.

a cartoon of a possible explanation. Defect band modeling [24,25] has shown that although peak defect densities in $Al_2O_3$ are lower, a partial overlap of the defect bands induces an almost uniform distribution of defect levels around the InGaAs conduction band edge, $E_c$. On the contrary, $HfO_2$ on InGaAs shows a minimum defect density slightly below the channel $E_c$ (~0.2 eV below $E_c$), which can be exploited for improving gate stack reliability by introducing an interface dipole. The assumption is that the IL layer gives rise to such a dipole shifting the defect levels up with respect to the InGaAs $E_c$ and shifting the minimum level into the device operating range. However, dipole engineering is not effective when a broad defect band without a clear minimum is present as is the case with $Al_2O_3$.

From the results shown till now, one can conclude that the 1 nm IL/3 nm $HfO_2$ stack shows an optimum for all electrical parameters although the $D_{it}$ and $N_{bt}$ levels are still above the targeted values (5 x $10^{11}$ /eV.cm$^2$ and 3 x $10^{10}$ /cm$^2$ respectively). However, when applying a PMA, we observe that the 1 nm IL/3 nm $HfO_2$ stacks degrades slightly i.e. a $D_{it}$, $\Delta N_{eff}$ increase and a reduction in the gamma value is observed in combination with a positive $V_{fb}$ shift (Fig. 4-shaded bars). On the contrary, the stack with the $Al_2O_3$ cap does not degrade when a PMA is added. This result implies that although the initial gate stack properties are degraded when adding an $Al_2O_3$ cap, this cap can help in stabilizing the gate stack upon a PMA.

In conclusion, the IL approach provides an improved interface quality and increases the misalignment between the InGaAs channel $E_f$ and the defect bands in the high-κ. The improved interface quality was proven to increase the performance of InGaAs MOS devices on both planar as well as nanowire architectures. However, the introduction of a cap layer is needed to provide a good thermal stability. Although $Al_2O_3$ can provide a higher stability for thermal processing, the unfavorable defect band distribution in the $Al_2O_3$ does not allow for dipole engineering. In the next part, we show that a $LaSiO_x$ cap can provide both an improved thermal stability and a more favorable defect band distribution.

### *3.2. Replacement of $Al_2O_3$ stabilization cap by $LaSiO_x$*

Fig. 6 shows the multi-frequency C-V for various gate stacks in Table I and demonstrates the impact of the insertion of $LaSiO_x$ between the IL passivation and $HfO_2$. All the dot capacitors were measured after PMA at 400°C in forming gas anneal for 5 minutes. Although the CV's from the 1 nm IL/3 nm $HfO_2$ stack (Fig. 6A) and the 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ stack (Fig. 6C) look similar, one can notice that the frequency dispersion is further reduced when $LaSiO_x$ is inserted between the IL and $HfO_2$. As was discussed in the previous section, an $Al_2O_3$ cap degrades the gate stack properties slightly. Although the difference between the stacks with the IL are subtle, a large difference can be observed when the IL is removed (Fig. 6C'). These results imply that both the IL and the $LaSiO_x$ cap are needed to optimize the gate stack properties.

The $D_{it}$, extracted at mid gap, and capacitance equivalent thickness (CET) are shown in fig. 7. The insertion of the IL (A) reduces the mid gap $D_{it}$ as was already reported in the previous section. The replacement of $Al_2O_3$ (B) by $LaSiO_x$ (C) further reduces the $D_{it}$ and a reduction of the CET is also observed (CET=1.55 nm, EOT=1.15 nm). In addition, the total density of charging oxide traps drops to a value close to 1 x $10^{10}$ /cm$^2$ at $E_{ox}$

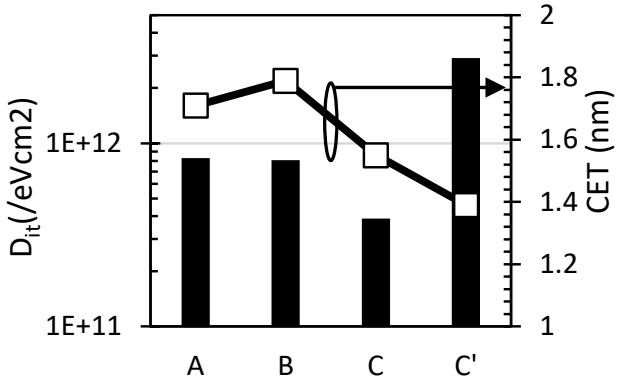


Figure 7: Mid gap $D_{it}$ (bars) and CET (dots) extracted from the C-V data presented in fig. 6. Replacement of $Al_2O_3$ (B) by $LaSiO_x$ (C) reduces the $D_{it}$ to less than 4 x $10^{11}$/cm$^2$eV. The CET drops to 1.55 nm.

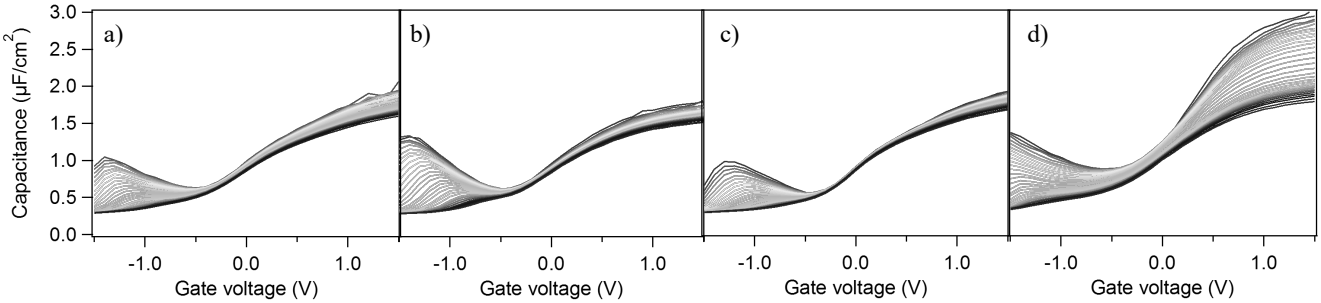


Figure 6. RT MF-CV's measured from dot capacitors of A) 1 nm IL/3 nm $HfO_2$, B) 1 nm IL/1 nm $Al_2O_3$/3 nm $HfO_2$, C) 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$, C') 1 nm $LaSiO_x$/3 nm $HfO_2$. Frequencies between 1 kHz-1 MHz (red-blue) were measured with logarithmic spacing. All capacitors received a PMA in forming gas for 5 minutes.

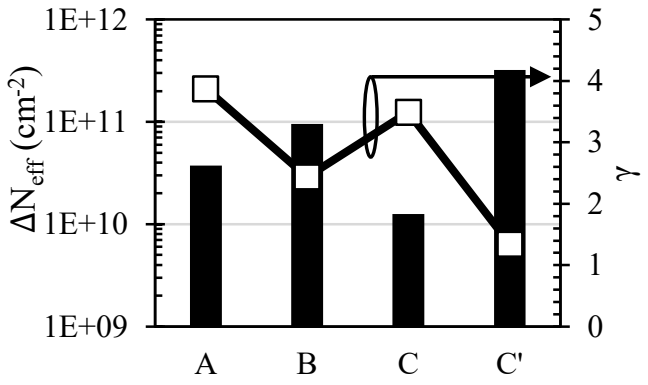


Figure 8: $\Delta N_{eff}$ (bars, left axis) extracted from C-V hysteresis ($V_{start}$=$V_{fb}$ - 0.5 V) by converting the measured $\Delta V_{fb}$ into an effective charge sheet at the interface by: $\Delta N_{eff}$=$\Delta V_{fb}$*$C_{ox}$/q, and reported at charging equivalent field of 3.5 MV/cm [6]. Field acceleration exponent, γ, (dots, right axis) i.e. the slope of the log-log plot $\Delta N_{eff}$ vs oxide field which is a measure of the misalignment between channel carrier energy-i.e. InGaAs $E_f$ and defect levels in the high-*k* [18].

= 3.5 MV/cm (Fig. 8) *meeting the target for 10 years operation* (10 years reliability criterion: $\Delta V_{fb}$ < 30 mV at 125°C. Assuming a typical time power law exponent of 0.13, the failure criterion projects $\Delta N_{eff}$ to less than 3 x $10^{10}$ /cm$^2$ at operating field, for an EOT of 1 nm). The reduction of oxide traps below the target level is the result of the combination of the IL layer and $LaSiO_x$ cap: while the IL layer increases the field dependence of the $\Delta N_{eff}$ (γ ~ 3.5), which is beneficial only for low voltage operation, the $LaSiO_x$ cap consistently reduces the density of charging defects irrespective of the operating voltage.

Fig. 9 shows the forward and backward sweep of gate voltage for the C-V hysteresis measured at different $V_{max}$ for 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ stack. At low overdrive voltages, the hysteresis is negligible. Only at higher overdrive voltages, a clear hysteresis can be measured. Notice also that the starting voltage for these measurements was carefully chosen at $V_{fb}$ - 0.5 V. As was reported in [25], the C-V hysteresis measurements can largely depend on the $V_{start}$ condition, as is also the case for gate stack under evaluation (Fig. 10). The more negative $V_{start}$ condition reflects the discharging of deep traps that can take place during OFF-state, when the device is biased deep into the depletion and is an equally important criterion to take into account. Measuring at $V_{start}$=$V_{fb}$ - 0.5 V shows that oxide trap densities are within target. Starting from a more negative $V_g$, the oxide trap density increases and γ decreases. This observation indicates that this gate stack has a low

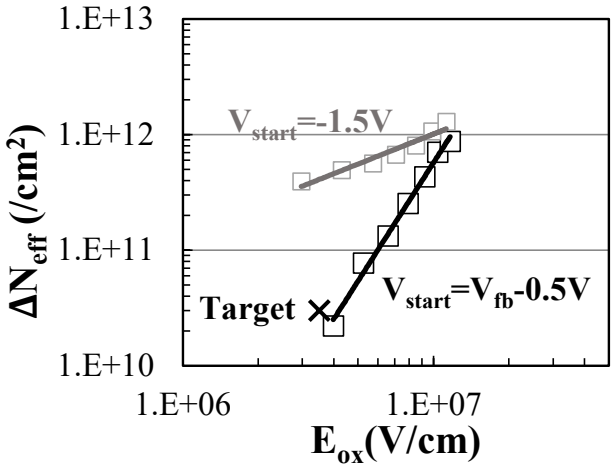


Figure 10: $\Delta N_{eff}$ as a function of applied $E_{ox}$ for the stack with 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ for 2 different $V_{start}$ conditions. $V_{start}$=-1.5V and $V_{start}$=$V_{fb}$-0.5V. The large dependence on the $V_{start}$ conditions points to the presence of deep traps i.e. located at energies below InGaAs $E_f$ at flatband.

amount of electron traps, but a more negative $V_{start}$ charges hole traps, thereby increasing the total amount of traps during the measurement and decreasing the voltage dependence.

Therefore, BTI measurements were performed at both positive and negative stress conditions to capture the max $V_{ov}$ for both stress conditions (Fig. 11). From these CV-BTI measurements, one can see that the 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ stack meets the

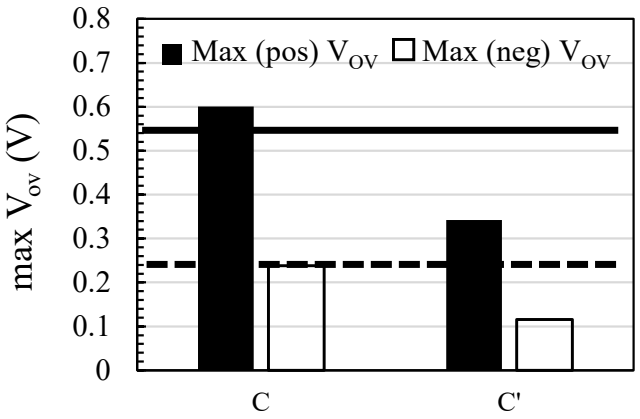


Figure 11: Max $V_{ov}$ measured from positive and negative CV-BTI on MOS capacitors. For a target $V_{DD}$=0.8V, the max pos $V_{ov}$ target (full line) is 0.53V and the max neg $V_{ov}$ target (dashed line) is -0.26V (i.e. 1/3*$V_{DD}$).

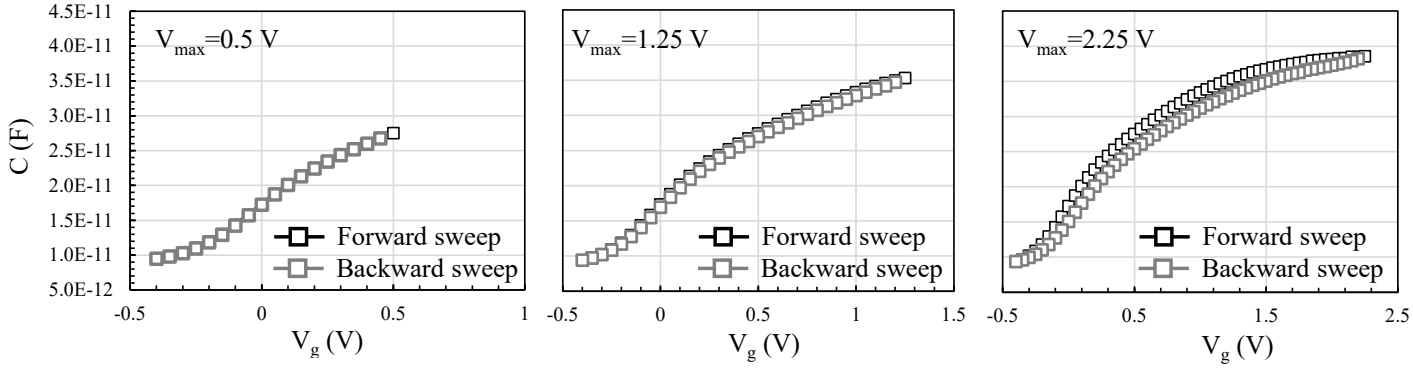


Figure 9. 100 kHz CV up and down traces of the 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ gate stack measured at 3 different $V_{max}$. $V_{start}$ was $V_{fb}$-0.5V.

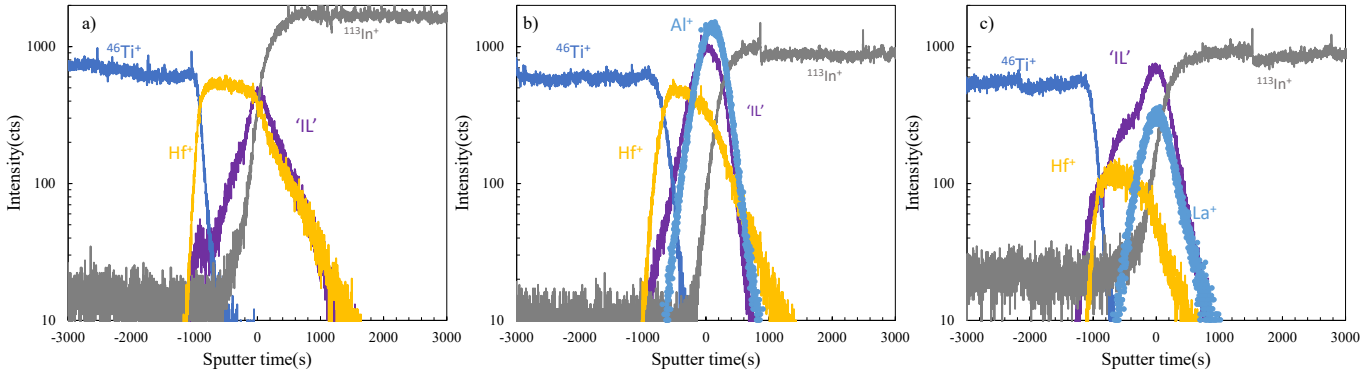


Figure 12. TOFSIMS positive ion profiles from MOSCAPs of stacks a) A, b) B and c) C from Table I. All layers are aligned at the peak of the IL atom profile.

max $V_{ov}$ target (for a $V_{DD}$=0.8 V) for both stress conditions. When removing the IL layer, none of the targets are met. As III-V materials will be introduced in technologies operating at $V_{DD}$=0.5V and resulting target $V_{ov}$=0.33 V (=2/3*$V_{DD}$), this implies that these MOSCAP $In_{0.53}Ga_{0.47}As$ devices with the 1 nm IL/1 nm $LaSiO_x$/3 nm $HfO_2$ gate stack surpass the IIIV reliability requirements.

Stabilization of the IL by the $Al_2O_3$ or $LaSiO_x$ cap is confirmed from the TOFSIMS profiles measured on dot capacitors that received a PMA (Fig. 12**)**. These profiles show the mixing of the Al atoms (from the $Al_2O_3$) or La atoms (from the $LaSiO_x$) with the IL. Diffusion of the IL atoms down into the InGaAs substrate is clearly present if no cap layer is deposited between IL and the $HfO_2$ (Fig. 12a). When an $Al_2O_3$ or $LaSiO_x$ cap is added on top of the IL (Figs. 12b and 12c) , a steep slope of the IL elements down into the substrate is observed. The hypothesis is that the mixing of the Al or La atoms with the IL atoms is increasing the stability of the IL. Although the chemistry from both $Al_2O_3$ and $LaSiO_x$ cap layers can provide stabilization of the interaction of the IL with the substrate, the electrical characteristics of the $LaSiO_x$ cap are more favorable.

Modeling of the shallow and deep defect bands using the approach as described in [26], was done and explains the effect of the $LaSiO_x$ cap **(**Fig. 13**)**. The introduction of the IL layer narrows the distribution of the shallow defect band as well as shifts the mean energy of that band to shallower energies. Adding $LaSiO_x$ in between the IL and $HfO_2$ further reduces the charging defect density. This reduction can be attributed to the stabilization that is provided by the $LaSiO_x$ cap.

### *3.3. MOSFET device characteristics*

Figs. 14 and 15 show the $I_{ds}$-$V_{gs}$ and $g_m$-$V_{gs}$ curves of the devices fabricated with stacks B ($Al_2O_3$ cap) and C ($LaSiO_x$ cap). Excellent device characteristics in the form of high $I_{on}/I_{off}$ ratio (> $2x10^6$, > $8x10^5$ at $V_{ds}$=0.05 V and 0.5 V respectively) and low $SS_{lin}$ (< 75 mV/dec) were extracted for both the gate stacks. The device characteristics for stacks B, C, C', and C'' are given in Fig. 16 and 17. The on-state current increases (Fig. 16a and b**)** and the $SS_{lin}$ decreases (Fig. 17) when $Al_2O_3$ (B) is replaced by $LaSiO_x$ (C) between the IL layer and $HfO_2$. When scaling the $HfO_2$ to 2 nm (C''), a CET of 1.46 nm (EOT of 1.06 nm) is achieved with a

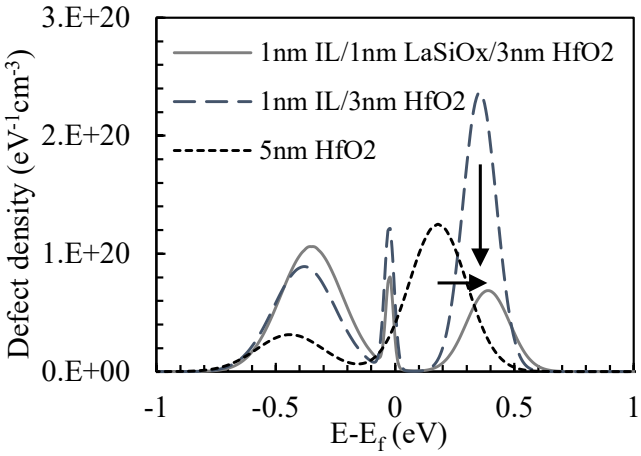


Figure 13**:** Defect density profile obtained by modeling the $\Delta V_{th}$ vs $V_{gate}$ as described in [25]. Insertion of the IL layer causes narrowing of the shallow defect band, thus enhancing γ and shifting the mean defect level of this band to shallower energy [19] but increases the density of defects at deeper energies. Insertion of $LaSiO_x$ consistently reduces the total defect density (both shallow and deep energies).

further improvement in the on-characteristics, and with a reduction in the $SS_{lin}$ to 68 mV/dec. Note that the stack without the IL layer (1 nm $LaSiO_x$/3 nm $HfO_2$ stack only, C'), exhibits high on-current compared to the stack with the 1 nm IL/1 nm $Al_2O_3$/3 nm $HfO_2$ but

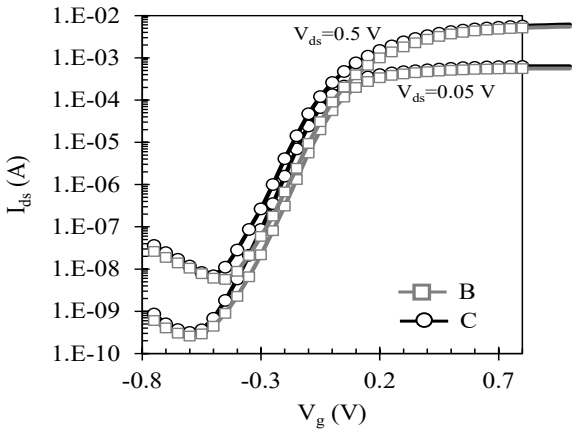


Figure 14**:** $I_{ds}$-$V_{gs}$ for $L_g$=10 µm, W=100 µm device.

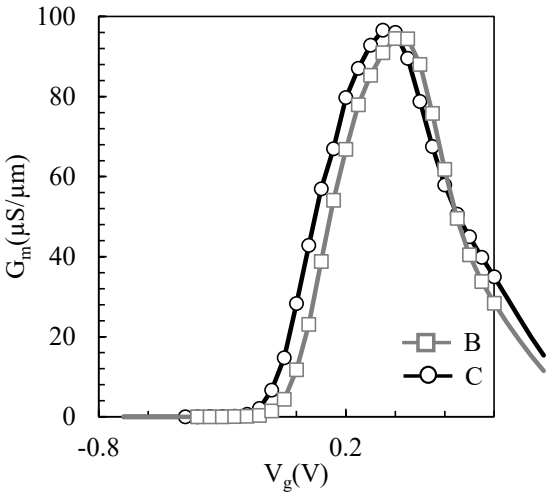


Figure 15: $G_m$-$V_{gs}$ for $L_g$=10µm, W=100µm device.

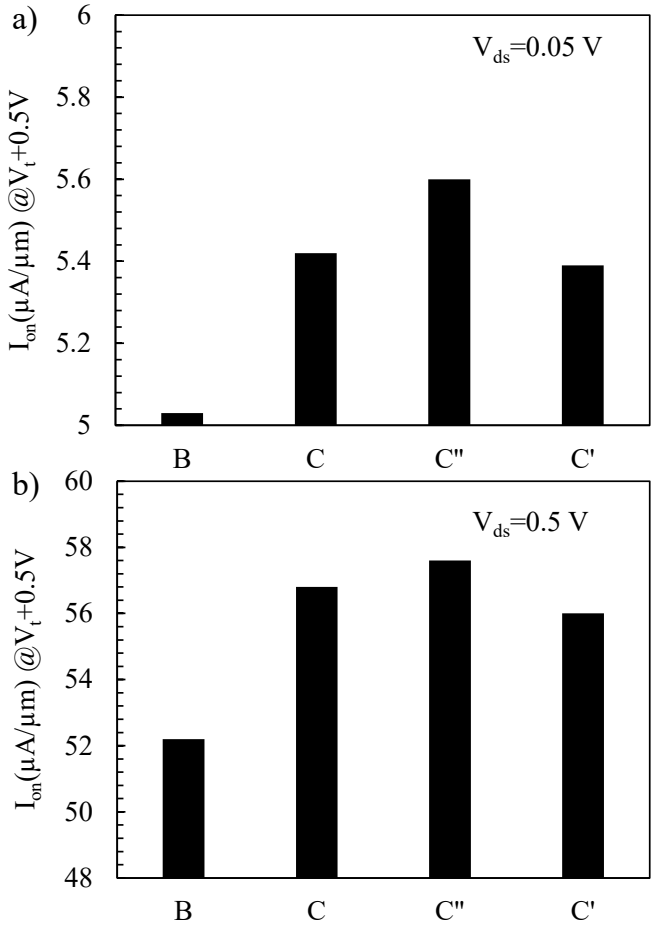


Figure 16: $I_{on}$ extracted at $V_t$+0.5V and for $V_{ds}$=0.05V (a) and $V_{ds}$=0.5V (b), W of the devices = 100µm, Lg=10µm. Replacement of $Al_2O_3$ (B) by $LaSiO_x$ (C) in the gate stack improves $I_{on}$. Further improvement can be seen when the gate stack is scaled down (C'').

also a high $SS_{lin}$ reflecting a higher mid gap $D_{it}$ extracted from the MOS capacitor C-V's (Fig. 7 and 8). Only slight changes in $V_{th\_lin}$ (~50 mV) are observed when changing the stabilization cap (Fig. 18).

The mobility data (Fig. 19) reveal that while the dominant

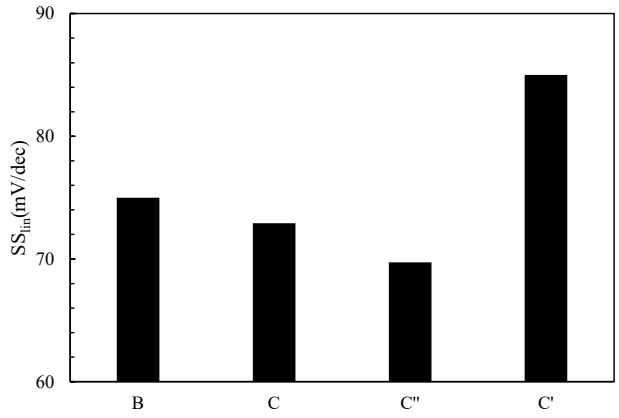


Fig. 17 $SS_{lin}$ for various gate stacks. Lg=50 µm. $SS_{lin}$ reduces by replacing $Al_2O_3$ (B) with $LaSiO_x$ (C) in the gate stack. Scaling the $HfO_2$ (C'') thickness leads to further reduction.

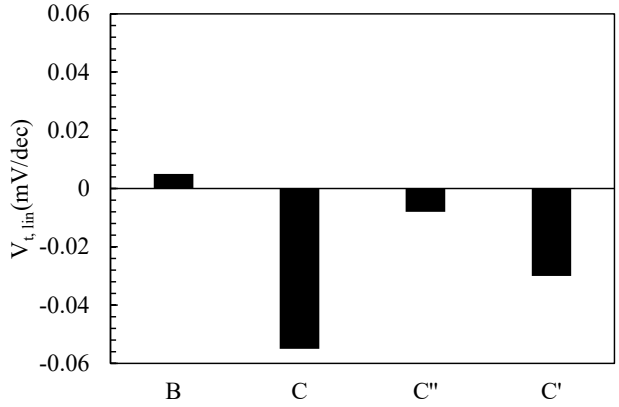


Figure 18 $V_{t,lin}$ for various gate stacks. $L_g$=50 µm. Slight $Vt_{lin}$ reduction by replacing $Al_2O_3$ (B) with $LaSiO_x$ (C) in the gate stack is observed.

impact of insertion of the IL layer is on the peak mobility ($\mu_{eff}$ at peak = 3531 $cm^2$/V.s), the replacement of the $Al_2O_3$ by $LaSiO_x$ increases the electron mobility at high charge carrier density.

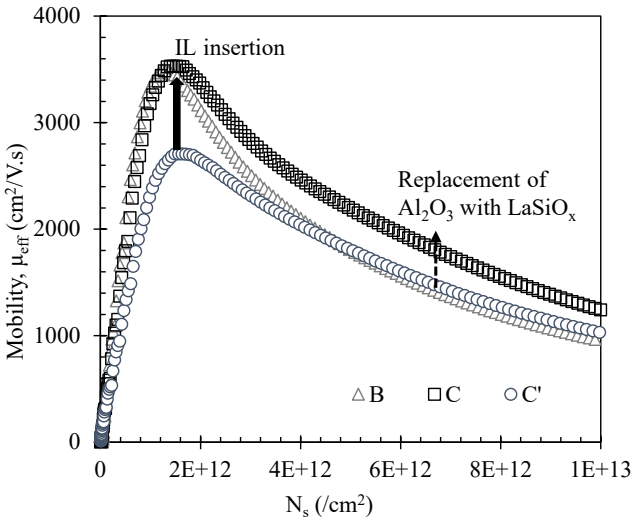


Figure 19 Improvement in the mobility at low $N_s$ (due to the introduction of IL) and high $N_s$ (as a result of replacement of $Al_2O_3$ with $LaSiO_x$). Mobility was extracted from $L_g$=50 µm devices.

This observation suggests a reduction in the roughness using $LaSiO_x$ in the gate stack instead of $Al_2O_3$. In addition, BTI measurements on MOSFETs confirm the good reliability observed on simple MOS capacitor structures. $\Delta N_{eff}$ and γ values were extracted under both positive and negative stress conditions (Fig. 20). Under both stress conditions, we can observe a reduction of $\Delta N_{eff}$ when adding the IL layer and further reduction is achieved by insertion of the $LaSiO_x$ cap. In parallel, the value of γ increases when adding the IL layer but levels off when inserting the $LaSiO_x$. This confirms both the

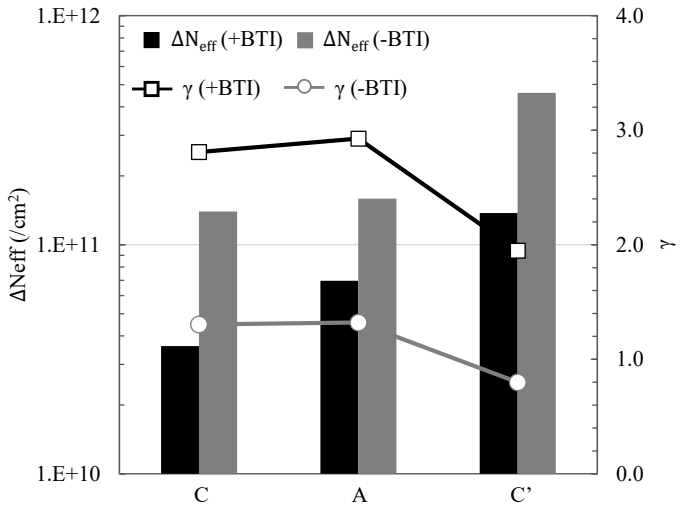


Figure 20 $\Delta N_{eff}$ and γ extracted from BTI measurements on MOSFETs applying both positive and negative stress conditions. The data from MOSFETs confirm the trends observed on MOSCAPs.

observation in measurement data and modeling results from the MOSCAP data i.e. the IL layer provides the misalignment between the defect levels in the high-κ and the InGaAs $E_f$ while the $LaSiO_x$ reduced the total charging oxide defects. At negative stress conditions, the differences are less pronounced.

The extrapolated max $V_{ov}$ and $V_{un}$ at 10 years are shown in Fig. 21. Benchmarking the max $V_{ov}$ of the newly proposed gate stack against Si gate stacks (Fig. 22) shows that by using the optimized gate stack III-V devices can meet even the more stringent reliability targets used for a scaled Si technology.

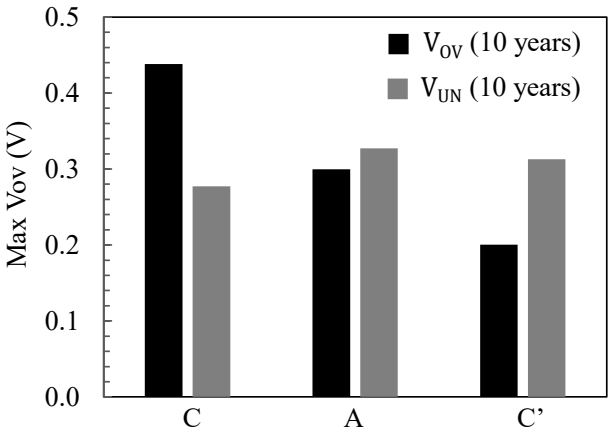


Figure 21. Max $V_{ov}$ and $V_{un}$ from BTI measurements on MOSFETs with different gate stacks.

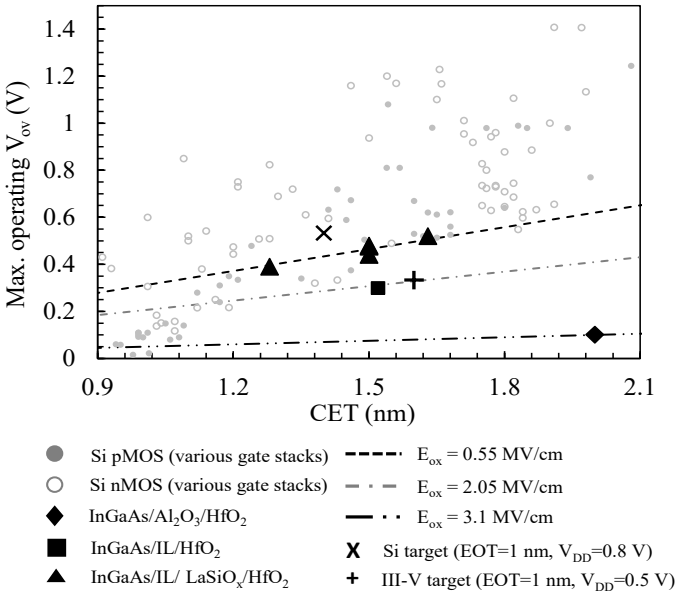


Figure 22. Max. operating overdrive voltage as a function of CET for various gate stacks on Si (p- and n-MOS) and InGaAs. The devices with the IL/$LaSiO_x$/$HfO_2$ gate stack surpass the relability target for III-V semiconductor based technology.

## 4. Conclusions

We have shown in this work the improved interface and reliability properties of the IL layer. A $D_{it}$ and $\Delta N_{eff}$ reduction are accompanied with a negative $V_{fb}$ shift and an increase in the value of γ. This suggests the formation of an interface dipole. When a favorable defect band distribution is present as is the case for $HfO_2$, dipole engineering can be applied to misalign the defect band with the InGaAs channel $E_f$. However, the thermal stability of this stack is limited and a severe intermixing of the IL layer with the InGaAs substrate at typical thermal budget of a IIIV gate stack, degrades the initial improvement seen from the IL layer.

A cap is needed to stabilize this interaction and both $Al_2O_3$ and $LaSiO_x$ can act as a stabilization layer by La or Al mixing with the IL-layer atoms. While the physical properties are very similar, the electrical properties in terms of oxide traps are very different. The different behavior can be explained by the presence of a broad defect band in $Al_2O_3$ making this cap layer not suitable for dipole engineering. On the other hand, $LaSiO_x$ shows a more favorable defect band distribution and a further reduction of the oxide defects is observed. In addition, the interface properties are improved and low CET (~1.5 nm) was maintained.

Excellent device characteristics were demonstrated combining the IL passivation layer with the bi-layer stack consisting of 1 nm $LaSiO_x$/3 nm $HfO_2$. III-V devices with record mobility and record reliability performance at scaled EOT were demonstrated. In addition, we show that this stack can be further scaled down to 1nm EOT without loss of performance or reliability.

### Conflict of Interest

The authors declare no conflict of interest.

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