

Tunable Resistorless Phase Shifter Realization with a Single VDGA

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ARTICLE INFO

Article history:

Received: 30 January, 2023

Accepted: 12 May, 2023

Online: 12 June, 2023

Keywords:

Voltage Differencing Gain

Amplifier (VDGA)

Phase shifter

Electronically tunable

All-pass filter

Voltage-mode circuit

ABSTRACT

This paper describes the design of a phase shifter with electrically adjustable parameters employing only one voltage differencing gain amplifier (VDGA) and one floating capacitor. This circuit requires no external resistors, resulting in a resistorless design and a low component count. The proposed circuit implements a first-order all-pass filter response with electronic control of its passband gain, pole frequency, and phase difference via bias current modification. Non-ideal effects of the VDGA on the phase shifter circuit are also examined. PSPICE simulation results using TSMC 0.25- μm real process parameters and practical test results using readily available LM13700s are incorporated to validate the theoretical conclusions. The results indicate that the simulations and experiments yielded phase shift deviations of 2.22% and 3.11%, respectively. The pole-frequency errors for simulations and experiments were 0.31% and 0.63%, respectively. The applicability of the suggested phase shifter is illustrated by the design of the voltage-mode quadrature oscillator.

1. Introduction

The design and synthesis of the phase shifter circuit, also known as a first-order all-pass filter, has received a great deal of interest [1]. In general, the phase behavior of the phase shifter circuit can be adjusted from 0° to 180° or from 180° to 0° , while its amplitude remains unchanged over the entire frequency range of interest. Due to this, the phase shifter circuit is employed in a number of communication and instrumentation systems, such as universal biquad filters, high quality factor frequency-selective filters, and quadrature and multiphase oscillators [2]-[20]. However, voltage-mode phase shifter circuits with one or more active components are the most often suggested circuits in [2]-[3], [5]-[16], [18]-[20]. Additionally, many of the works in [2]-[3], [5], [10]-[16], [18],[20] are inaccessible electronically. Moreover, all of these configurations are realized with the use of external passive resistors.

The main objective of this contribution is, therefore, to design a simple and compact phase shifter circuit with only one active and one passive component. Without an extra passive resistor, the

suggested structure consists merely of one voltage difference gain amplifier (VDGA) and one floating capacitor. The benefits of the design include the facility, low power consumption, and small integrated chip area. Furthermore, the important features of the proposed phase shifter, including passband gain (H_0), pole frequency (ω_p), and phase response (ϕ), are electronically tunable through the transconductance gains of the VDGA. A thorough investigation is also done into the non-ideal gain effects of the VDGA on the circuit performance. In addition, a new voltage-mode quadrature oscillator is proposed to highlight the advantages of the designed phase shifter. The designed circuit and its application are simulated using PSPICE software using TSMC 0.25- μm CMOS process technology, and the simulation results are consistent with the theoretical analysis. The experimental measurement results from the laboratory breadboard using commercially available LM13600s are also given to prove the features of the proposed circuit. In addition, a summary of the performance comparison of the proposed circuit and those that the previous works [2]-[20] is provided in Table 1. The observations show that the suggested circuit has more features than recently published circuits, which is commendable.

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Table 1: Comparative study of the proposed circuit with the similar previous works.

Ref	Year	No. of active components	No. of passive components	Resistorless structure	Variable-gain control	Electronic tunability	Power dissipation (W)	Pole frequency (Hz)	Supply voltages (V)	Technology
[2]	2005	CCII+ = 2	R = 2, C = 2	no	yes	no	NA	15.9 k	±12 (experiment)	AD844
[3]	2006	DDCC = 1	R = 1, C = 1	no	no	no	NA	265.4 k	±3.3 (simulate)	1.2 μm
[4]	2017	MMCC = 1, CFA = 1	R = 1, C = 1	yes	no	yes	NA	9.91 M	NA	AD835, AD844
[5]	2000	CDBA = 1	R = 1, C = 1	no	no	no	NA	1.59 M	±2.5 (simulate)	0.8 μm
[6]	2001	CCCII+ = 1	R = 1, C = 1	yes	no	yes	NA	10 M	±2.5 (simulate)	0.35 μm
[7]	2015	VDGA = 1	R = 1, C = 1	yes	yes	yes	1.45 m	429 k	±1.5 (simulate)	0.35 μm
[8]	2017	VDBA = 1	R = 1, C = 1	yes	no	yes	0.37 m	1.06 M	±0.75 (simulate)	0.25 μm
[9]	2019	LT1228 = 1	R = 2, C = 1	yes	no	yes	NA	100 k	±5 (simulate)	LT1228
[10]	2010	FDCCH = 1	R = 2, C = 1	no	no	no	NA	1.59 M	±3.3 (simulate)	0.35 μm
[11]	2012	DDCC = 2	R = 1, C = 1	no	no	no	NA	15.91 M	±2.5 (simulate)	0.5 μm
[12]	2011	FDCCH = 1	R = 1, C = 1	no	no	no	NA	2.65 M	±1.3 (simulate)	0.35 μm
[13]	2012	DDCC = 2	R = 1, C = 1	no	no	no	NA	1.17 M	±2.5 (simulate)	0.5 μm
[14]	2019	Fig.2: CFOA = 2 Fig.3: CFOA = 3	Fig.2: R = 5, C = 1 Fig.3: R = 6, C = 1	no	yes	no	Fig.2: 0.26, Fig.3: 0.39	7.59 k	±10 (experiment)	AD844
[15]	2020	VCII+ = 2	R = 3, C = 1	no	yes (TM)	no	1.22 m	636.6 k	±0.9 (simulate)	0.18 μm
[16]	2020	EXCCII = 1	R = 2, C = 2	no	no	no	0.7 m	3.18 M	±1.2 (simulate)	0.25 μm
[17]	2021	ICCI+ = 2	Fig.2: R = 1, C = 1 Fig.3: C = 1	Fig.2: no, Fig.3: yes (active resistor)	no	Fig.2: no, Fig.3: yes	3.29 m (simulate)	7.96 M (simulate), 159 k (experiment)	±0.75 (simulate), ±9 (experiment)	0.13 μm, AD844
[18]	2021	CFOA = 2	Fig.1: R = 3, C = 1 Fig.2: R = 4, C = 1	no	yes	no	NA	33.829 k	±8 (simulate/ experiment)	AD844
[19]	2021	FDCCH = 1	C = 1	yes (active resistor)	no	yes	2 m	6.37 M	±1.25 (simulate)	0.25 μm
[20]	2022	DVCC = 2	Fig.1 : R = 1, C = 1 Fig.2 : R = 3, C = 1	no	Fig.1: no Fig.2: yes	no	0.6	62.41 k	±5 (simulate)	AD844
This work	2022	VDGA = 1	C = 1	yes	yes	yes	1.56 m (simulate)	1.59 M (simulate), 159 k (experiment)	±0.75 (simulate), ±5 (experiment)	0.25 μm, LM13600

Abbreviation:

NA = Not Available

CCII = second-generation current conveyor, DDCC = differential difference current conveyor, MMCC = Multiplication Mode Current Conveyor, CFA = current feedback operational amplifier, CDBA = current differencing buffered amplifier, CCCII+ = plus-type current-controlled current conveyor, VDBA = voltage differencing buffered amplifier, FDCCH = fully differential current conveyor, CFOA = current feedback operational amplifier, VCII+ = plus-type second-generation voltage conveyor, EXCCII = extra-X second generation current conveyor, ICCII+ = plus-type second-generation current conveyor, DVCC = differential voltage current conveyor, TM = transimpedance-mode

2. Proposed Circuit Configuration

The VDGA was first introduced in [21], as illustrated in Figure 1. The VDGA device is a six-port versatile active building block described by the following matrix equation [21]-[22]:

$$\begin{bmatrix} i_z \\ i_{zc} \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} g_{mA} & -g_{mA} & 0 \\ -g_{mA} & g_{mA} & 0 \\ 0 & 0 & -g_{mB} \\ 0 & 0 & \beta \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad (1)$$

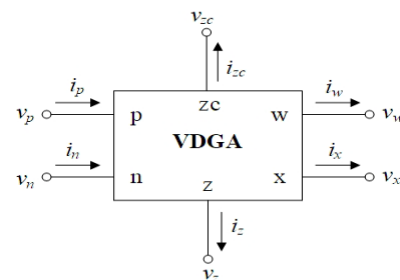


Figure 1: Circuit symbol of the VDGA.

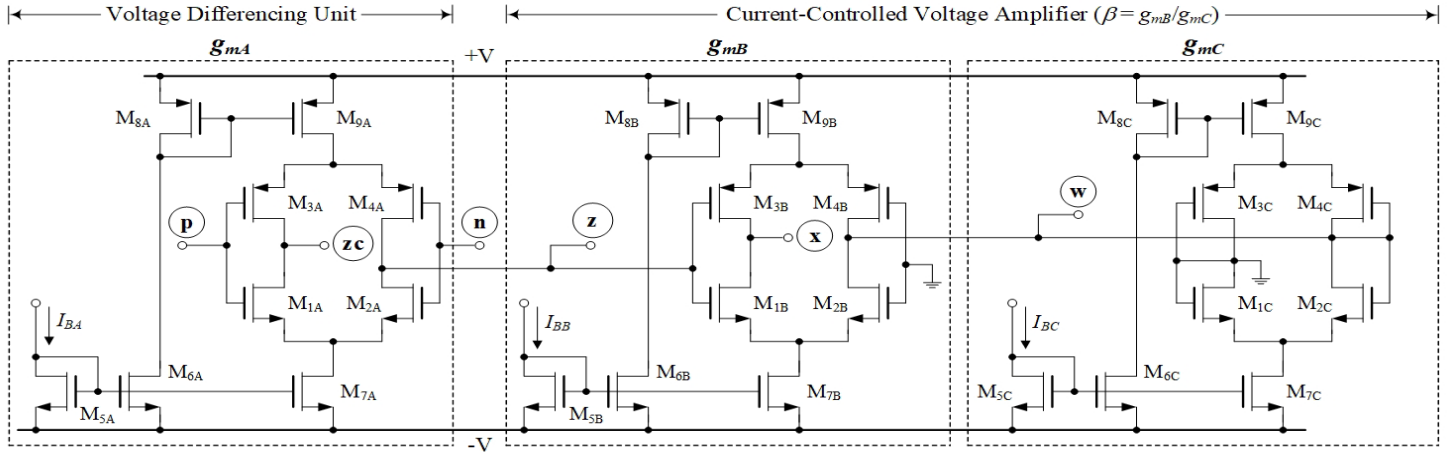


Figure 2: CMOS internal structure of the VDGA.

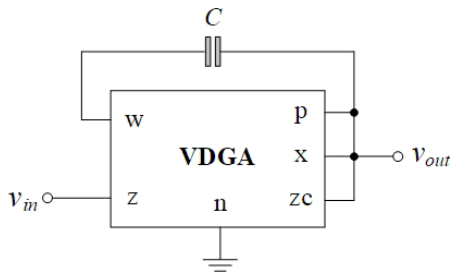


Figure 3: Proposed single VDGA-based resistotless phase shifter circuit.

In (1), g_{mk} ($k = A, B, C$) and β represent the transconductance gain and the voltage transfer gain of the VDGA, respectively. This element has two high input impedance voltages (v_p and v_n), three high output impedance currents (i_z , i_{zc} and i_x), and a zero output impedance voltage (v_w).

The values of g_{mk} and β , when implemented in CMOS technology such as that depicted in Figure 2 [22]-[23], can be expressed as follows:

$$g_{mk} = \sqrt{K \left(\frac{W}{L} \right) I_{Bk}} \quad (2)$$

and
$$\beta = \frac{g_{mB}}{g_{mC}} \quad (3)$$

where $K = \mu_0 C_{ox}$ is the transistor transconductance, μ_0 is the carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W/L is the width-to-length ratio of the transistor. From Figure 2, the CMOS VDGA is made up of three sections of transconductance amplifiers ($M_{1A} - M_{9A}$, $M_{1B} - M_{9B}$ and $M_{1C} - M_{9C}$). Each transconductor contributes its own transconductance gain g_{mk} that is electronically controllable. Consequently, external bias currents I_{Bk} can be used to adjust the parameters g_{mk} and β of the VDGA.

Figure 3 depicts the realization of the phase shifter circuit that requires only one VDGA and one floating capacitor without an external resistor requirement. Despite the fact that the capacitor C employed in this realization is floating, a second poly-layer technique is provided by advanced integrated circuit (IC) technology, making it simple to implement [24]. A preliminary

analysis of the proposed configuration in Figure 3 gives the voltage transfer function shown below

$$\frac{V_{out}(s)}{V_{in}(s)} = \beta \left(\frac{\frac{sC}{g_{mC}} - 1}{\frac{sC}{g_{mA}} + 1} \right) \quad (4)$$

Assuming $g_m = g_{mA} = g_{mC}$, the passband gain (H_0), pole frequency (f_p) and phase response (ϕ) of the configuration are obtained as:

$$H_0 = \beta \quad (5)$$

$$f_p = \frac{\omega_p}{2\pi} = \frac{g_m}{2\pi C} \quad (6)$$

and
$$\phi = \pi - 2 \tan^{-1} \left(\frac{\omega C}{g_m} \right) \quad (7)$$

Thus, the transconductances g_{mk} or by changing the external bias currents I_{Bk} can be modified to alter the values of H_0 , ω_p and ϕ . Also noticed is the fact that the gain β can be controlled to provide orthogonal H_0 control.

3. Effects of Non-Ideal Gains

Ideally, the VDGA features are thought to be perfect. However, due to device mismatch, transfer errors may occur in CMOS implementations of VDGA, deviating from the expected behavior. The impact of the VDGA non-idealities on the functioning of the suggested circuit must thus be investigated. In view of VDGA's non-ideal gains, (1) may be changed and expressed as:

$$\begin{bmatrix} i_z \\ i_{zc} \\ i_x \\ v_w \end{bmatrix} = \begin{bmatrix} \alpha_A g_{mA} & -\alpha_A g_{mA} & 0 \\ -\alpha_A g_{mA} & \alpha_A g_{mA} & 0 \\ 0 & 0 & -\alpha_B g_{mB} \\ 0 & 0 & \delta \beta \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \end{bmatrix} \quad (8)$$

where $\alpha_k = 1 - \varepsilon_\alpha$ represents the transconductance inaccuracy coefficient, and $\delta = 1 - \varepsilon_\delta$ represents the parasitic voltage transfer

gain. Here, ε_α ($|\varepsilon_\alpha| \ll 1$) and ε_δ ($|\varepsilon_\delta| \ll 1$) are the undesirable parameters deviating from unity due to the transfer errors of the VDGA. For the non-ideal analysis of the suggested phase shifter circuit in Figure 3, the modified parameters H_0 , f_p , and ϕ can be given by the following expressions:

$$H_0 = \delta\beta \quad (9)$$

$$f_p = \frac{\alpha_A g_m}{2\pi C} \quad (10)$$

and
$$\phi = \pi - 2 \tan^{-1} \left(\frac{\delta\omega C}{\alpha_B g_m} \right) \quad (11)$$

It is evident from (9)-(11) that the circuit parameters H_0 , f_p and ϕ are slightly affected by the unwanted factors α_k and δ of the VDGA. However, this effect can be diminished by modifying the transconductance gain g_{mk} for the circuit shown in Figure 3. According to (2), the value of g_{mk} can be modified conveniently by altering the external bias current I_{Bk} .

4. Simulation Verification

In order to evaluate the performance of the proposed phase shifter circuit in Figure 3, the CMOS-based VDGA in Figure 2 was simulated with the TSMC 0.25- μm transistor model in PSPICE computer simulation program. Symmetrical supply voltages of $+V = -V = 0.75\text{V}$ were used to bias the VDGA. The transistor sizes (W and L) used in the VDGA realization are listed in Table 2.

Table 2: Transistor sizes used in VDGA realization of Figure 2.

Transistor	W (μm)	L (μm)
$M_{1k}\text{-}M_{2k}$	15	0.25
$M_{3k}\text{-}M_{4k}$	23	0.25
$M_{5k}\text{-}M_{7k}$	4.5	0.25
$M_{8k}\text{-}M_{9k}$	5.5	0.25

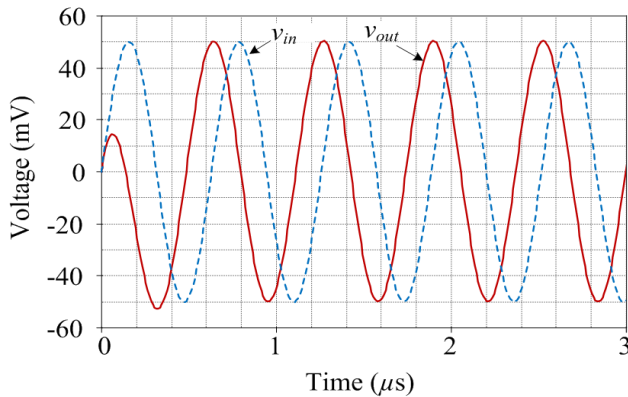


Figure 4: Simulation results of the transient waveforms of the proposed phase shifter in Figure 3.

The active and passive component values are specified as: $g_{mA} = g_{mB} = g_{mC} = 1 \text{ mA/V}$, ($I_{BA} = I_{BB} = I_{BC} = 100 \mu\text{A}$), and $C = 0.1 \text{ nF}$ for the proposed resistorless phase shifter with $H_0 = 1$ and $f_p = 1.59 \text{ MHz}$. Figure 4 shows the simulated transient responses of the proposed circuit for an input signal with a sinusoidal frequency of 1.59 MHz and an amplitude of 50 mV (peak). In contrast to the

theoretical value of $\phi = 90^\circ$, the simulation results show a phase difference between v_{in} and v_{out} of $\phi = 92^\circ$.

Figure 5 also shows the simulation outcomes for the gain and phase frequency characteristics in comparison to the ideal curves. The simulated f_p is approximately 1.585 MHz , resulting in a frequency error of 0.31% . The simulation results clearly show that they closely match the theoretical predictions, demonstrating the usefulness of the suggested circuit. It is discovered that the simulated power dissipation of the circuit is around 0.82 mW , when the input v_{in} is kept grounded.

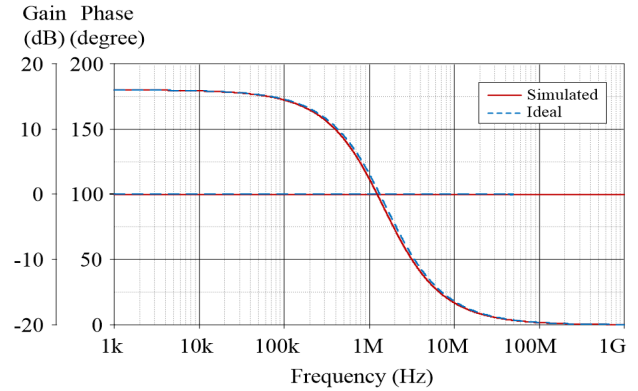


Figure 5: Ideal and simulated frequency characteristics of the proposed phase shifter in Figure 3.

Figure 6 depicts the electronic tuning of H_0 without altering the ϕ -value by controlling the g_{mB} -value. The values of the circuit components for these settings are listed in Table 3. The sinusoidal input waveform in these figures is 20 mV (peak) at $f = 1.59 \text{ MHz}$. While $g_{mA} = g_{mC} = 1 \text{ mA/V}$ ($I_{BA} = I_{BC} = 100 \mu\text{A}$) remains constant, the values of g_{mB} are altered between 0.707 mA/V , 1 mA/V , and 1.414 mA/V ($I_{BB} = 50 \mu\text{A}$, $100 \mu\text{A}$, and $200 \mu\text{A}$). These facts lead to the β -value being, respectively, 0.707 , 1 , and 1.414 .

Table 3: Component values for electronic tuning of H_0 with I_{BB} .

I_{BB} (μA)	g_{mB} (mA/V)	$I_{BA} = I_{BC}$ (μA)	$g_{mA} = g_{mC}$ (mA/V)	β (g_{mB}/g_{mC})
50	0.707	100	1	0.707
100	1.000	100	1	1.000
200	1.414	100	1	1.414

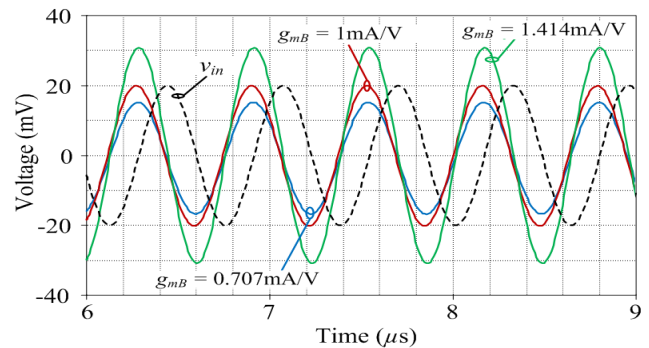


Figure 6: Simulated transient waveforms of the proposed phase shifter with tuning g_{mB} value.

The simulated transient responses of the circuit and its corresponding phase response are also shown in Figures 7 and 8 for three different values of g_m , i.e., $g_m = g_{mk} = 0.707 \text{ mA/V}$, 1 mA/V and 1.414 mA/V ($I_{Bk} = 50 \mu\text{A}$, $100 \mu\text{A}$, and $200 \mu\text{A}$). The computed values of ϕ were determined to be, respectively, 70.5° , 90° , and 109.4° . The measured ϕ values based on the simulation results were 73° , 92.1° , and 110.2° , respectively, which accord quite well with the estimated values.

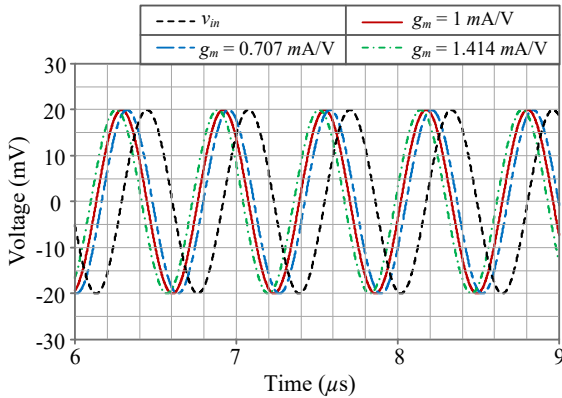


Figure 7: Simulated transient waveforms of the proposed phase shifter with tuning g_m value.

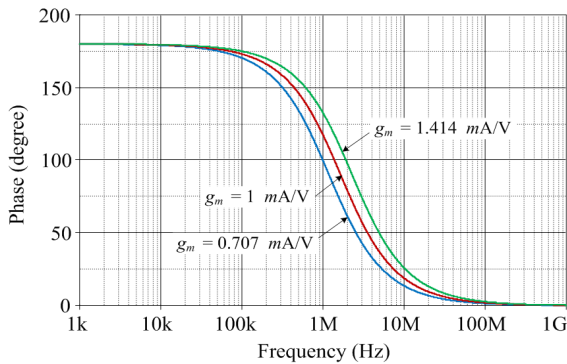


Figure 8: Simulated frequency characteristics of the proposed phase shifter with tuning g_m value.

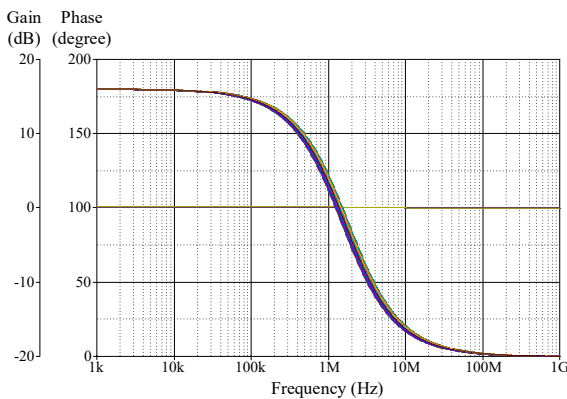


Figure 9: Monte Carlo statistical analysis for the frequency responses of the proposed phase shifter circuit with 5% capacitor tolerance.

In order to demonstrate the impact of capacitor tolerance on the gain and phase responses, a Monte Carlo analysis with a hundred runs is performed for the proposed phase shifter circuit given in

Figure 3. It is supposed that the value of capacitor C will change uniformly by 5%. Figure 9 depicts the simulated frequency responses of Monte Carlo statistical analysis. In addition, the results of the Monte Carlo analysis indicate that the mean and sigma of f_p are approximately 1.589 MHz and 2.204×10^{10} , respectively. It can be clearly seen from Figure 9 that the capacitance tolerance has a minor effect on the frequency response of the proposed circuit.

5. Experimental Measurements

Experimental measurement was used to validate the practicability of the designed circuit in Figure 3. The schematic for the practical implementation of the VDGA is shown in Figure 10 [25], using readily available IC dual-OTA LM13600s from National Semiconductor [26]. For LM13600s, the DC bias voltages are $+V = -V = 5V$.

The proposed phase shifter circuit of Figure 3 was constructed with the following component values: $g_{mk} = 1 \text{ mA/V}$ ($I_{Bk} = 100 \mu\text{A}$) and $C = 1 \text{ nF}$. For time-domain analysis, the circuit was applied with a sinusoidal input of frequency 159 kHz and of amplitude 50 mV (peak). The measured waveforms for v_{in} and v_{out} are shown in Figure 11. The measured ϕ is 92.8° , which is close to the theoretical ϕ of 90° . Accordingly, the measured phase error is about 3.11%. Figure 12 also shows the measured Fourier spectrum of the output waveform v_{out} at 159 kHz .

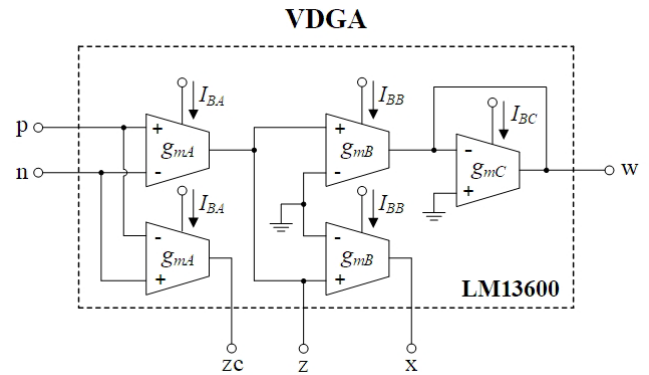


Figure 10: Practical realization of VDGA using readily available IC LM13600s

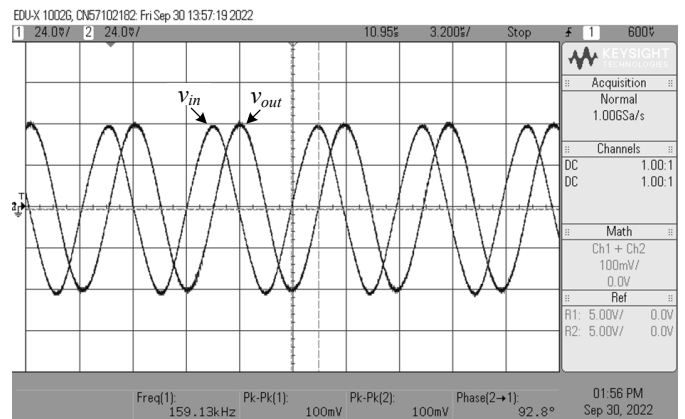


Figure 11: Measured time-domain waveforms of v_{in} and v_{out} for the propose circuit in Figure 3.

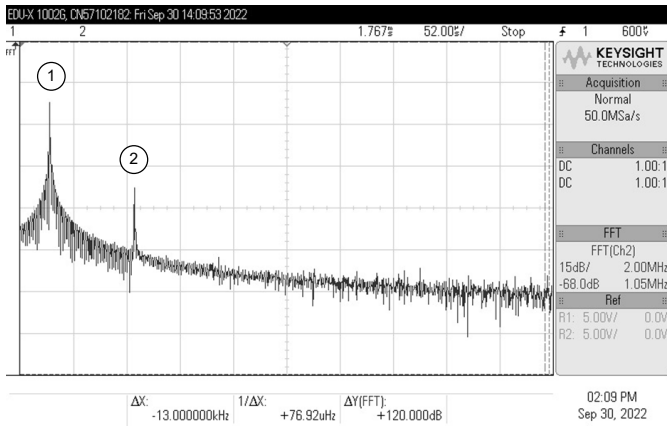


Figure 12: Measured spectrum frequency of v_{out} at 159 kHz (No.1: Frequency = 159 kHz, Gain = -28.91 dB, and No.2: Frequency = 479 kHz, Gain = -29.13 dB)

The next observation on the circuit is carried out on its frequency response characteristic. The measured frequency responses in comparison to the theoretical responses are given in Figure 13. The measured value of f_p is found to be 158 kHz, which corresponds to the frequency deviation of 0.63%. The experimental testing results show that while the gain response is essentially constant up to the working frequency of roughly 4 MHz, the phase characteristic is found to change with frequency, as predicted. The difference between measured and ideal curves in the high-frequency region is predominantly attributable to the gain-bandwidth product of the IC OTA LM13600s used to implement the circuit [26]. Obviously, higher-speed active devices could produce superior frequency responses.

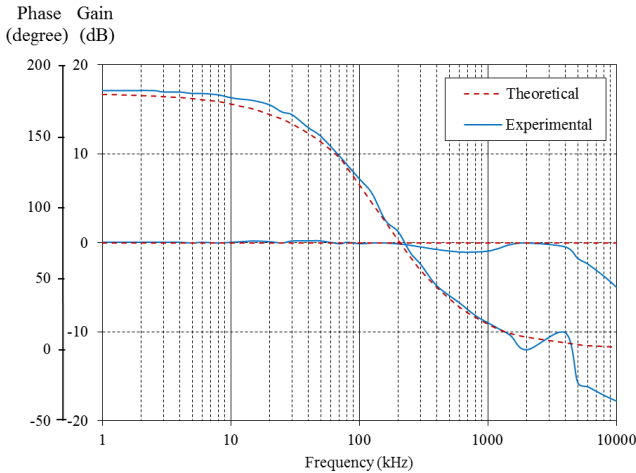


Figure 13: Theoretical and measured frequency responses of the propose circuit in Figure 3.

6. Quadrature Oscillator Application

The quadrature oscillator (QO) circuit can be simply implemented by utilizing the proposed phase shifter circuit, as shown in Figure 14. In the configuration, VDGA2 and C_2 create a simple lossless integrator. The following relationship describes the characteristic equation of the QO circuit:

$$s^2 + g_{mA1} \left(\frac{1}{C_1} - \frac{\beta_1}{C_2} \right) s + \left(\frac{g_{mA1} g_{mB1}}{C_1 C_2} \right) = 0 \quad (12)$$

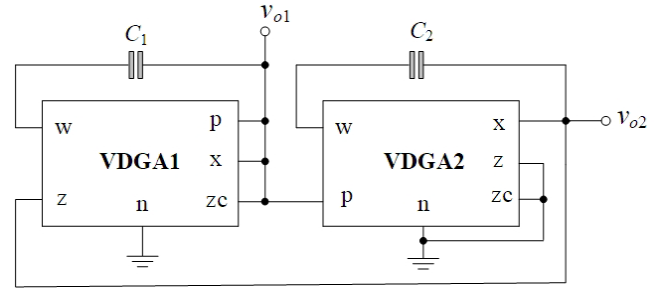


Figure 14: Quadrature oscillator implemented with the proposed circuits.

From the characteristic equation in (12), the condition for oscillation (CO) is satisfied at

$$\frac{\beta_1 C_1}{C_2} \geq 1 \quad (13)$$

and the frequency of oscillation (f_o) is obtained as:

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi} \sqrt{\frac{g_{mA1} g_{mB1}}{C_1 C_2}} \quad (14)$$

The equation for the relationship between the produced quadrature signals is

$$\frac{V_{o2}(j\omega)}{V_{o1}(j\omega)} = \left| \frac{g_{mA1}}{\omega C_2} \right| e^{j90^\circ} \quad (15)$$

Obviously, both quadrature voltages v_{o1} and v_{o2} are ideally shifted by a phase (ϕ) of 90° . It may also be observed that g_{mA1} and C_2 have a direct impact on the amplitude ratio of the quadrature voltages. Therefore, it follows that the output voltage amplitude of the QO can be controlled by the values of g_{mA1} and C_2 . When the frequency is altered, equal voltage amplitudes can be achieved by changing g_{mA1} while maintaining C_2 .

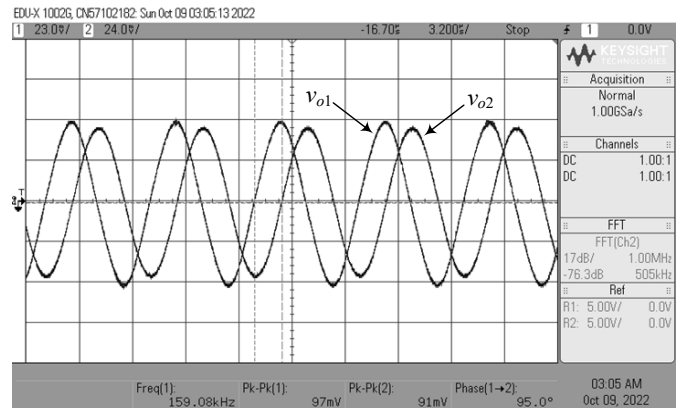


Figure 15: Measured waveforms of the developed QO circuit at v_{o1} and v_{o2} outputs.

The following values were chosen for the circuit elements in order to test the functionality of the QO circuit in Figure 14. The selection of $g_{mk} = 1 \text{ mA/V}$ ($I_{Bk} = 100 \mu\text{A}$) and $C_1 = C_2 = 1 \text{ nF}$ for all transconductances and capacitances results in $f_o = 159 \text{ kHz}$. Figure 15 shows the typical waveforms measured at v_{o1} and v_{o2}

output terminals with $f_o = 159.08$ kHz and $\phi = 95^\circ$. The resulting deviations for f_o and ϕ are 0.05% and 5.55%, respectively. The differences from ideal values are mainly attributed to the non-ideal gains and parasitic elements of IC LM13600s, which are described in Section 3. In Figure 16, the corresponding Lissajous figure of the QO circuit is also shown. Figure 17 illustrates the measured spectrum frequency of v_{o2} of the QO circuit, with the corresponding frequencies and gains at various spectra listed in Table 4. All the results support the practical usefulness of the proposed phase shifter circuit in implementing the quadrature oscillator.

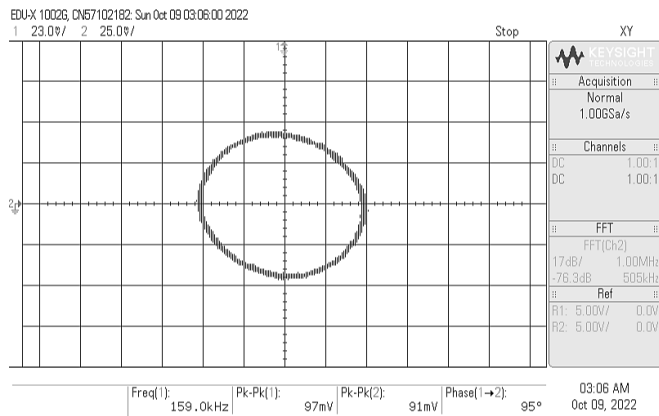


Figure 16: Lissajous figure of the developed QO circuit in Figure 14.

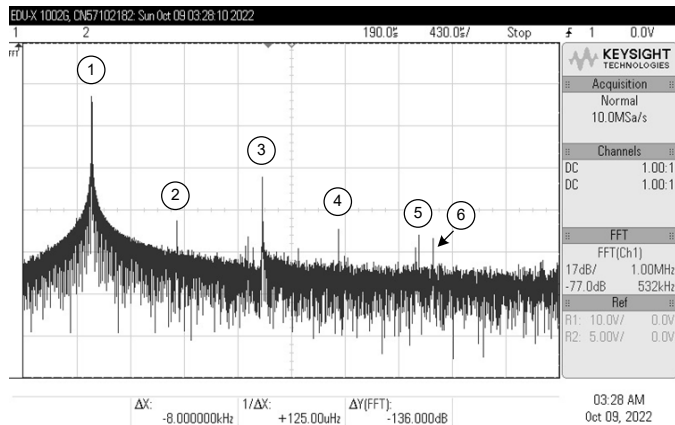


Figure 17: Measured spectrum frequency of v_{o2} at 159 kHz.

Table 4: Frequencies and gains at different spectrums of Figure 17.

No.	Frequency (kHz)	Gain (dB)
1	159	-30.798
2	318	-79.650
3	478	-63.720
4	620	-86.022
5	770	-88.677
6	796	-89.208

7. Conclusions

The paper describes the design of the compact resistorless tunable phase shifter circuit. The described phase shifter circuit requires only one VDGA as an active component and one floating capacitor, resulting in a resistorless architecture and ease of integration. Electronic tuning of the important features of the resulting design, such as the passband gain (H_0), pole frequency (f_p)

and phase response (ϕ), is possible by modifying the g_m -values of the VDGA. The non-ideal analysis of the VDGA was also carried out. The voltage-mode quadrature oscillator has been used as an illustrative application for the proposed design. PSPICE simulation data with TSMC 0.25- μ m CMOS model parameters have been performed to support the theoretical research. In addition to validating the practical circuit behaviors, experimental measurements with commercially available IC LM13600s have been included.

Conflict of Interest

The authors declare no conflict of interest.

Acknowledgments

This work was supported by King Mongkut's Institute of Technology Ladkrabang [2566-02-01-041]. The Institute of Research and Development Rajamangala University of Technology Isan, and the Faculty of Engineering, Rajamangala University of Technology Isan, Khonkaen Campus, are also acknowledged for their providing support.

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