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Active Simulation of Grounded Parallel-Type Immittance Functions Employing VDBAs and All Grounded Passive Components

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ABSTRACT

This communication proposes a grounded immittance function simulator that, depending on the proper choice of the passive components, can simulate parallel-type impedances of the R-L, R-C, and L-C forms. Only two grounded passive components and two voltage differencing buffered amplifiers (VDBAs) are used to implement the suggested circuit. All three simulated equivalent elements, namely R_{eq}, L_{eq}, and C_{eq}, can be electronically adjusted through the VDBA's transconductance gain. The impact of the non-ideality of the VDBA device on the developed simulator is examined in detail. The voltage-mode bandpass filter has been implemented using the suggested active LC parallel impedance simulator to show that it performs as predicted. To prove the theory, the proposed circuit is simulated using the PSPICE tool. The findings of the experimental measures are also presented to demonstrate the circuit's feasibility.

1. Introduction

Electronic devices have assimilated into our daily lives in the world today. The development of novel technologies will be influenced by the published findings. In several analog signal processing solutions, the different active devices, such as current conveyor (CC), operational transconductance amplifier (OTA), current feedback operational amplifier (CFOA), and current differencing buffered amplifier (CDBA), have gained widespread attention. Similarly, since 2008, the voltage differencing buffered amplifier (VDBA) has been recognized as one of the most versatile and practical devices [1]-[2].

The VDBA element has a tunable transconductor as the input section and a voltage buffer as the output section. Because of this feature, this active element can be used in a variety of voltage-mode, current-mode, and mixed-mode analog circuits and applications [2–6]. Passive elements, such as resistors, capacitors, and inductors, were used in a variety of applications, including analog active filter circuits, sinusoidal oscillator design, and impedance cancellation circuit. However, when applied in the implementation of an integrated circuit (IC), the behavior of passive elements was constrained by its enormous size and suffered from electronic tuning properties. As a consequence, an IC that mimicked the behavior of a passive element was implemented using an active element [7-9]. The parallel-type R-L simulators that were suggested in the literature [10–12] needed at least three active components. Similar to that, three or more passive components are required to realize the circuits in [11–12]. The circuits in [13] also need a high-voltage operation.

Therefore, the contribution of this work is to propose a grounded parallel R-L, R-C, and L-C impedance simulator, which depends on the appropriate selection of the passive element being used. The suggested simulator circuit uses only two VDBAs, two grounded passive components, and allows electronically control of the equivalent simulated elements via the transconductance gains of the VDBAs. In this study, the VDBA non-ideality effect on the actual immittance simulator is examined. With 0.18-μm CMOS technology, the proposed R-L, R-C, and L-C impedance simulator circuit in frequency domain was simulated using PSPICE program. Time-domain analysis and temperature-dependent simulation are also carried out in the parallel R-C simulator. The theoretical analysis is validated by experimental laboratory measurements using commercially available IC LT1228. Additionally, the active L-C simulator has also been used to apply a second-order voltage-

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mode bandpass filter in order to validate the viability. All results, both from simulations and experiments, are discovered to be in accordance with the theoretical predictions.

2. Fundamental of VDBA

Figure 1 depicts the electrical symbol of the VDBA element. This functional block has two input terminals (p and n) that meet high input impedance criteria and two output terminals (z and w), which have high and low impedances, respectively. Under ideal operating condition, the effective transconductance gain (g_m) of the VDBA converts the differential voltage between v_p and v_n (v_p - v_n) into an output current (i_z) at terminal z. The voltage drop (v_z) at the z terminal is transferred to the output voltage (v_w) at the w terminal. From its ideal operating condition, the following matrix equation can be used to characterize the terminal relationship of the VDBA [1-2]:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \quad (1)$$

In general, the g_m value in (1) can be changed by electronic means via the external bias voltage or current.

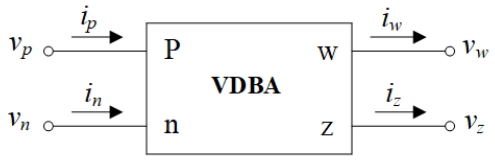


Figure 1: Schematic symbol of the VDBA.

In non-ideal assumption, the characteristic of VDBA can be modified as [3]:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} . \quad (2)$$

In above expression, $\alpha = (1 - \varepsilon_{gm})$ and $\beta = (1 - \varepsilon_v)$, where $|\varepsilon_{gm}| << 1$ and and $|\varepsilon_v| << 1$ stand for transconductance inaccuracy coefficient and the voltage tracking error, respectively.

A CMOS model of VDBA consisting of the differential amplifiers with active load (M_1-M_4 and M_7-M_{10}), and the source follower (M_{11}) is shown in Figure 2. For the CMOS VDBA in Figure 2, the relationship between g_m and the bias current I_B can be characterized as follows [4]:

$$g_m = \sqrt{\mu C_{ox} \left(\frac{W}{L}\right) I_B} . \quad (3)$$

Here, μ is the effective carrier mobility, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the effective channel width and length of M_1 and M_2 transistors, respectively.

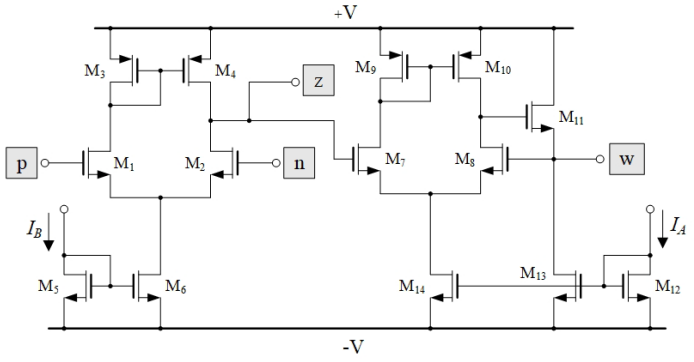


Figure 2: CMOS model of the VDBA used in this work.

3. Proposed Parallel-Type Immittance Function Simulator

According to Figure 3, the suggested grounded parallel-type immittance simulator is made up of two VDBAs and two grounded passive components. Based on ideal condition consumption, the input admittance (Y_{in}) of the circuit is derived as:

$$Y_{in} = \frac{i_{in}}{v_{in}} = g_{m1} g_{m2} Z_A + \frac{1}{Z_B} . \quad (4)$$

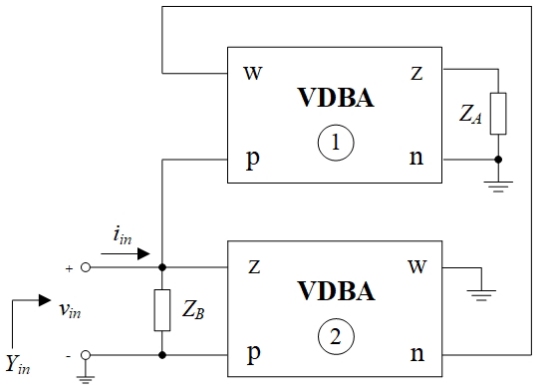


Figure 3: Proposed grounded parallel-type immittance function simulator.

The proposed parallel R-L, R-C, and L-C immittance simulator was made achievable by selecting the appropriate passive components, which describes the realized circuit. Its simulated impedances are summarized in Table 1, which illustrates that all synthetic simulator values can electronically be changed by the transconductance g_{mi} of the i-th VDBA (i = 1, 2). Since all of the passive components are grounded, the configuration is attractive from further integration point of view. Another attractive feature of the design is that it does not need any special component equality for its realization.

Under the non-ideal operation given in (2), the results of reevaluating the proposed circuit in Figure 3 can be summarized in Table 2.

Table 1: Equivalent Circuit and Corresponding Equivalent Values for Figure 3 in Ideal Case

Z_A	Z_B	Equivalent circuit	Equivalent values
$1/sC_A$	R_B	parallel R-L	$R_{eq} = R_B$,

			$L_{eq}=\frac{C_A}{g_{m1}g_{m2}}$
R_A	$1/sC_B$	parallel R-C	$R_{eq}=\frac{1}{R_A g_{m1}g_{m2}}$, $C_{eq}=C_B$
$1/sC_A$	$1/sC_B$	parallel L-C	$L_{eq}=\frac{C_B}{g_{m1}g_{m2}}$, $C_{eq}=C_A$

Table 2: Equivalent Element Values for Figure 3 in Non-Ideal Case

Z_A	Z_B	Equivalent circuit	Equivalent values
$1/sC_A$	R_B	parallel R-L	$R_{eq}=R_B$, $L_{eq}=\frac{C_A}{\alpha_1\alpha_2\beta_1 g_{m1}g_{m2}}$
R_A	$1/sC_B$	parallel R-C	$R_{eq}=\frac{1}{\alpha_1\alpha_2\beta_1 R_A g_{m1}g_{m2}}$, $C_{eq}=C_B$
$1/sC_A$	$1/sC_B$	parallel L-C	$L_{eq}=\frac{C_B}{\alpha_1\alpha_2\beta_1 g_{m1}g_{m2}}$, $C_{eq}=C_A$

The sensitivity coefficients of the simulated equivalent values, R_{eq} L_{eq} and C_{eq}, are each affected by the active and passive circuit components, and the finding values are produced as follows.

For parallel R-L;

$$S_{R_B}^{R_{eq}}=1\ ,\ S_{\alpha_1,\alpha_2,\beta_1,g_{m1},g_{m2}}^{L_{eq}}=-1\ ,\ S_{C_A}^{L_{eq}}=1\ . \qquad (5)$$

For parallel R-C;

$$S_{\alpha_1,\alpha_2,\beta_1,R_A,g_{m1},g_{m2}}^{R_{eq}}=-1\ ,\ S_{C_B}^{C_{eq}}=1\ . \qquad (6)$$

For parallel L-C;

$$S_{\alpha_1,\alpha_2,\beta_1,g_{m1},g_{m2}}^{L_{eq}}=-1\ ,\ S_{C_B}^{L_{eq}}=1\ ,\ S_{C_A}^{C_{eq}}=1\ . \qquad (7)$$

All of the sensitivity coefficients from above (5) to (7) have magnitudes that are less than or equal to one. As a result, the sensitivity of all the proposed parallel R-L, R-C, and L-C immittance simulators is quite low.

4. Simulation Results

PSPICE simulation program has been used to simulate the suggested grounded parallel-type impedance simulator in Figure 3. The simulator was designed employing CMOS VDBA of Figure 2 with a model of 0.18-µm process parameters from TSMC. Table 3 lists the computed aspect ratio (W/L) for each transistor. The supply voltages used to bias this circuit were +V= -V= 0.75 V.

Table 3: Calculated transistor dimensions of VDBA in Figure 2

Transistor	W/L (µm/µm)
M_1-M_2, M_5, M_7-M_8, M_{12}-M_{13}	2.4/0.18
M_3, M_9, M_{14}	5/0.18
M_4, M_{10}	5.2/0.18
M_6	3.25/0.18
M_{11}	10/0.18

The following components were chosen for simulations: I_{B1} = I_{B2} = 90 μA for $g_m = g_{m1} = g_{m2}$ = 0.641 mA/V, $R_A = R_B$ = 1 kΩ, and $C_A = C_B$ = 50 pF. Using data from Table 1, the simulated equivalent values of Figure 3 can be derived as:

- for R-L simulator: R_{eq} = 1 kΩ and L_{eq} = 0.12 mH;
- for R-C simulator: R_{eq} = 2.44 kΩ and C_{eq} = 50 pF;
- for L-C simulator: L_{eq} = 0.12 mH and C_{eq} = 50 pF.

The total power consumed in the circuit for this setting was found to be 0.388 mW.

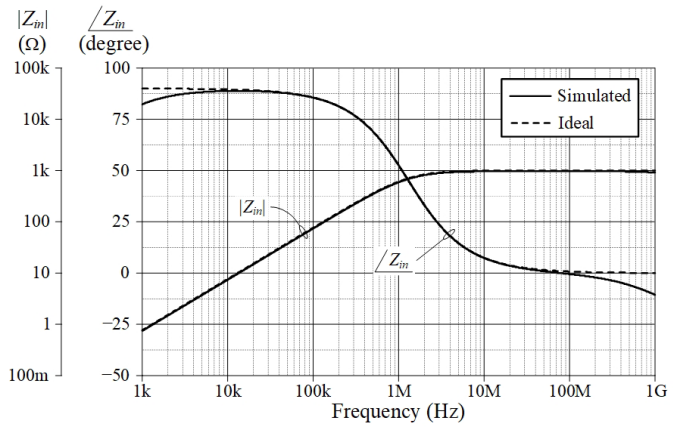
Based on the results of the simulation and theory, Figure 4 depicts the magnitude and phase frequency characteristics of the proposed parallel-type immittance simulator circuit in Figure 3. The frequency corners (f_c) of the R-L and R-C impedance simulators in Figs. 4(a) and 4(b) obtained from the simulation results are found to be roughly 1.29 MHz, which is pretty close to the calculated value of 1.30 MHz. In addition, the simulated f_c value of the L-C impedance simulator was discovered to be 2.04 MHz, which nearly equals to the ideal value of f_c = 2.05 MHz. The input voltage (v_{in}) and current (i_{in}) responses through the R-C impedance simulator are also displayed in Figure 5 as simulated time-domain waveforms. This performance was evaluated by supplying a sinusoidal input signal with a peak value of 50 mV at f = 1 MHz to the simulated RC impedance circuit.

In order to further illustrate the electronic adjustability of the proposed circuit, the parallel L-C simulator has been performed to change $I_B = I_{B1} = I_{B2}$ = 50 μA, 100 μA, and 200 μA, while maintaining $C_A = C_B$ = 50 pF. As a consequence, the simulated equivalent inductance value (L_{eq}) has been altered to 0.22 mH, 0.11 mH, and 54.8 μH, respectively, while the simulated equivalent capacitance value (C_{eq}) remains constant at 50 pF. The results of the simulated frequency responses compared with the theory are given in Figure 6.

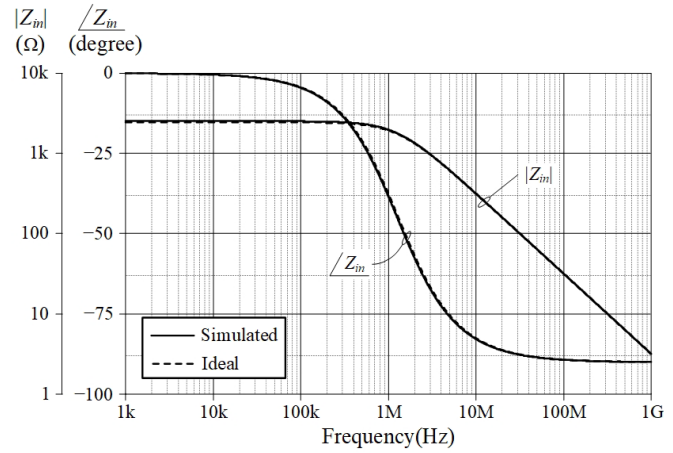
The impact of varying ambient temperature variation on the simulator responses is also being considered. This was accomplished by testing the proposed R-C simulator circuit with changes in ambient temperature ranging from 0˚C to 100˚C with steps of 25˚C. Figure 7 displays the result of its magnitude variations.

5. Experimental Results

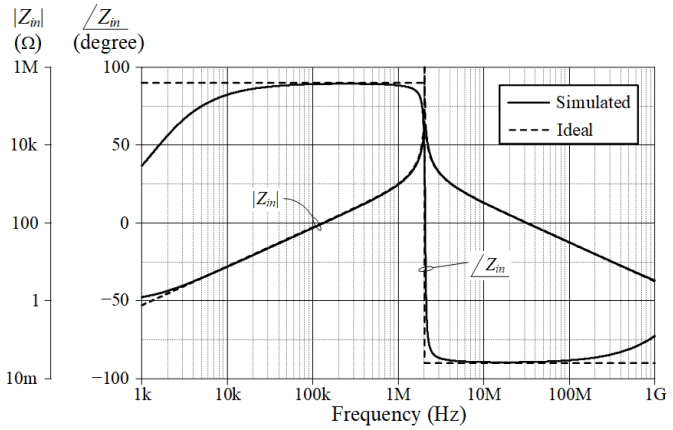
In order to further confirm the feasibility of the proposed idea, the suggested circuit of Figure 3 has been tested in the laboratory utilizing IC LT1228 from Linear Technology [14]. The package information and internal behavior of IC LT1228 are shown in Figure 8. There are two amplifiers: OTA and CFOA. The OTA is used to provide a high-impedance differential input and a current source output with wide output voltage compliance, while the CFOA is utilized to transmit voltage from the z terminal to the o terminal, and the current from the z terminal to the x terminal. According to the following relation, the transconductance gain (g_m) of the LT1228 in this case is reliant on the external bias current (I_B) [14]:



(a)



(b)



(c)

Figure 4: Ideal and simulated frequency responses of the proposed parallel-type immittance simulator circuit in Figure 3. (a) R-L impedance simulator (b) R-C impedance simulator (c) L-C impedance simulator

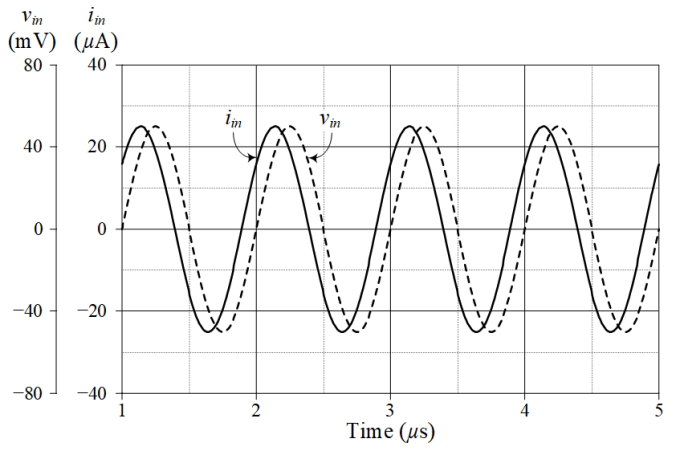


Figure 5: Simulated time-domain responses for v_{in} and i_{in} of the R-C simulator.

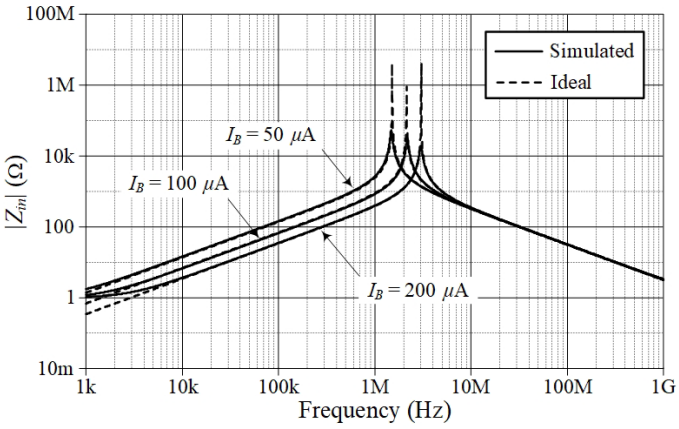


Figure 6: Simulated frequency responses of the L-C simulator with varying I_B.

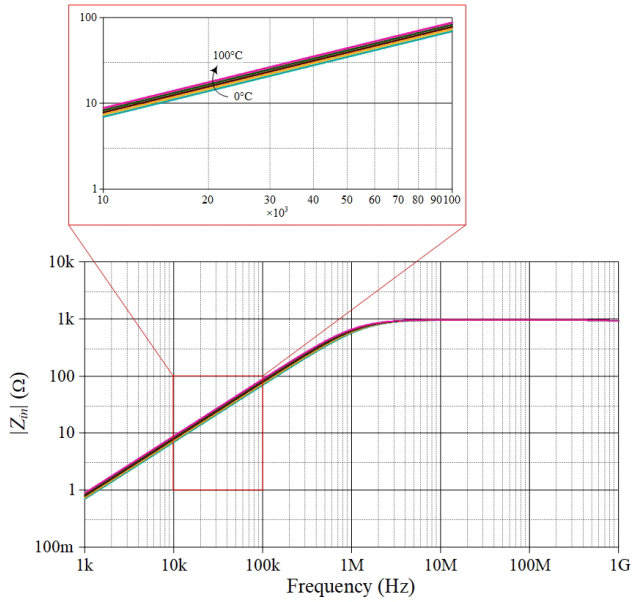
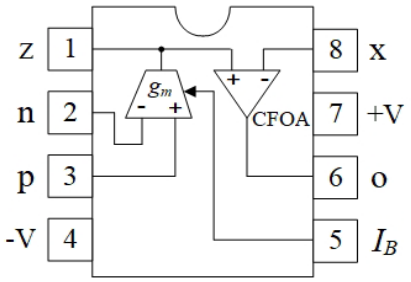


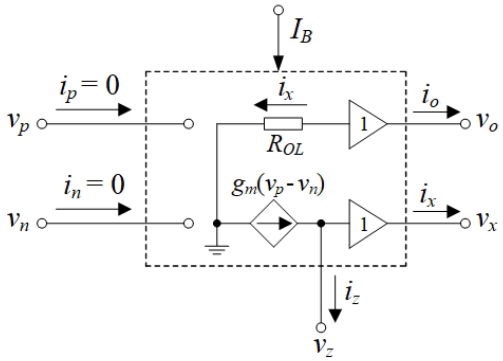
Figure 7: Simulated frequency responses of the R-C simulator at different temperature (0˚C, 25˚C, 50˚C, 75˚C, and 100˚C).

$$g_m = 10I_B \,. \tag{8}$$

In the case of parallel R-L impedance simulation, the active and passive components for the experimental measurement were taken as follows: $g_m = g_{m1} = g_{m2} = 0.5$ mA/V ($I_B = I_{B1} = I_{B2} = 50$ μA), $R_B = 1$ kΩ, and $C_A = 1$ nF, resulting in $R_{eq} = 1$ kΩ, and $L_{eq} = 4$ mH. With symmetrical supply voltages of ±5 V, the LT1228 was biased. Figure 9 shows the grounded parallel lossy inductor's measured magnitude and phase responses for the selected components.

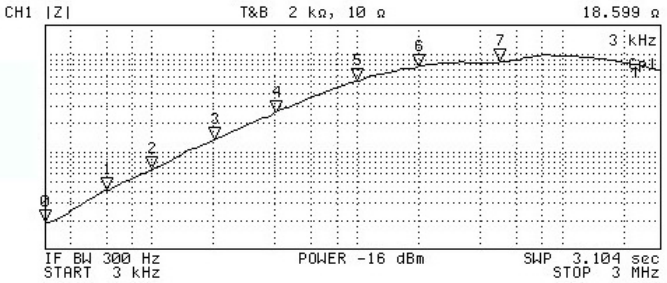


(a)



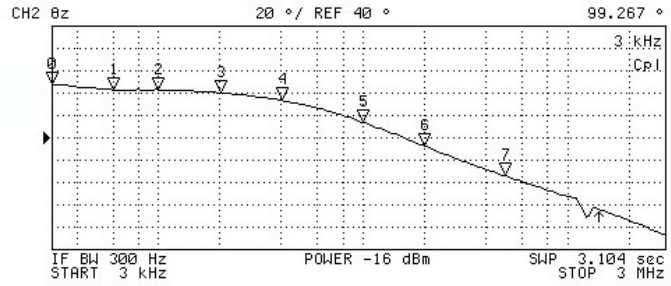
(b)

Figure 8: IC LT1228 (a) package information (b) its internal behavior.



N	SWP PARAM	VAL
0	3 kHz	18.599 Ω
1	6 kHz	40.525 Ω
2	10 kHz	65.485 Ω
3	20 kHz	132.23 Ω
4	40 kHz	251.76 Ω
5	100 kHz	536.14 Ω
6	200 kHz	751.61 Ω
7	500 kHz	838.94 Ω

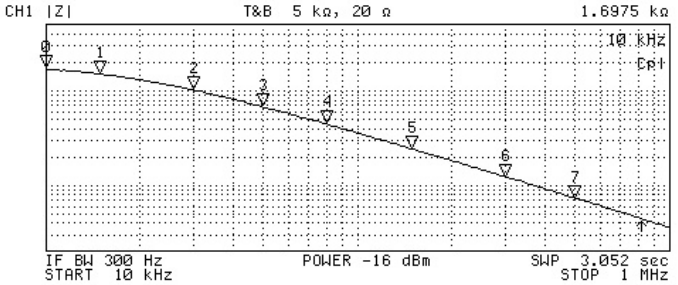
(a)



N	SWP PARAM	VAL
0	3 kHz	94.267 °
1	6 kHz	82.793 °
2	10 kHz	83.121 °
3	20 kHz	80.294 °
4	40 kHz	73.487 °
5	100 kHz	53.942 °
6	200 kHz	32.572 °
7	500 kHz	5.8288 °

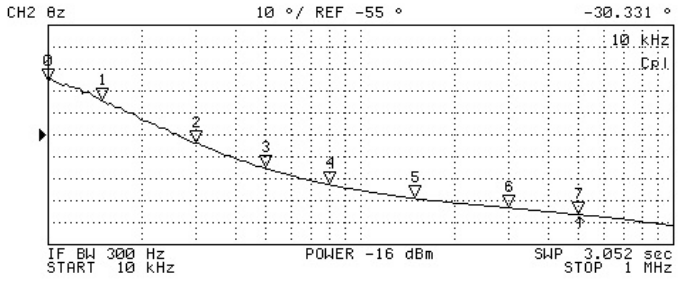
(b)

Figure 9: Measured frequency responses of the parallel R-L simulator (a) magnitude response (b) phase response



N	SWP PARAM	VAL
0	10 kHz	1.6975 kΩ
1	15 kHz	1.4837 kΩ
2	30 kHz	1.0093 kΩ
3	50 kHz	670.32 Ω
4	80 kHz	439.41 Ω
5	150 kHz	240.99 Ω
6	300 kHz	122.06 Ω
7	500 kHz	72.889 Ω

(a)



N	SWP PARAM	VAL
0	10 kHz	-30.331 °
1	15 kHz	-39.565 °
2	30 kHz	-58.712 °
3	50 kHz	-70.298 °
4	80 kHz	-77.599 °
5	150 kHz	-83.904 °
6	300 kHz	-88.317 °
7	500 kHz	-91.252 °

(b)

Figure 10: Measured frequency responses of the parallel R-C simulator (a) magnitude response (b) phase response

The parallel R-C simulator was then tested with the following parameters: $g_m = g_{m1} = g_{m2} = 1$ mA/V ($I_B = I_{B1} = I_{B2} = 100$ µA), $R_A = 500$ Ω, and $C_B = 4.7$ nF, yielding $R_{eq} = 2$ kΩ, and $C_{eq} = 4.7$ nF. Figure 10 shows the measured frequency responses for the equivalent input impedance of the simulator. The experimental results shown in Figures 9 and 10 demonstrate the suggested circuit's practicality in application areas.

6. Application Example

The second-order voltage-mode bandpass filter in Figure 11(a) is intended to emphasize operational performance as an illustration of an application. The bandpass filter realization utilizing the proposed L-C parallel immittance simulator in Figure 3 is shown in Figure 11(b). The voltage transfer action of the filter is written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s\left(\frac{1}{RC_{eq}}\right)}{s^2 + s\left(\frac{1}{RC_{eq}}\right) + \frac{1}{L_{eq}C_{eq}}} \quad . \tag{9}$$

The natural angular frequency (ω_o) and the quality factor (Q) of the filter in Figure 11 are determined from (9), respectively, by:

$$\omega_o = 2\pi f_o = \sqrt{\frac{1}{L_{eq}C_{eq}}} \quad , \tag{10}$$

and

$$Q = R\sqrt{\frac{C_{eq}}{L_{eq}}} \quad . \tag{11}$$

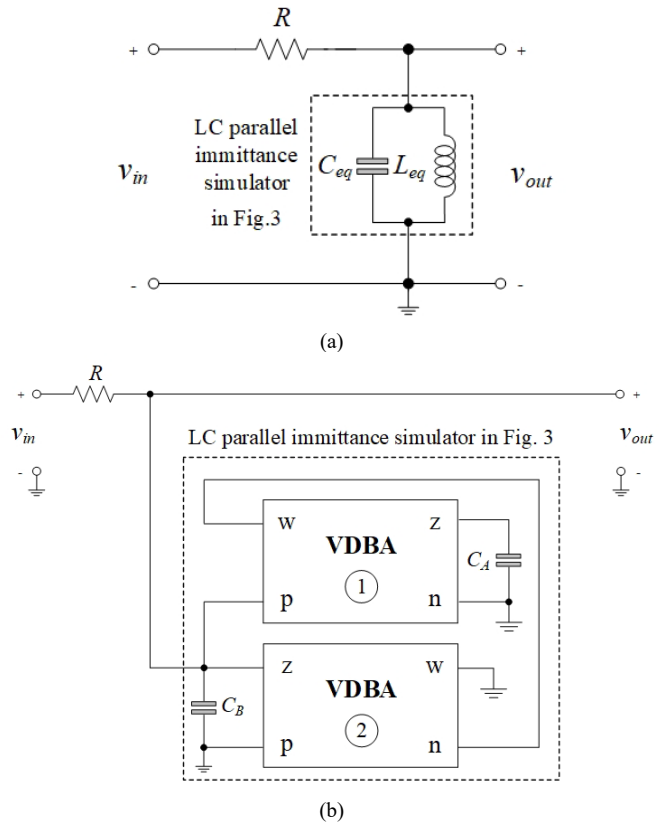


Figure 11: Second-order voltage-mode bandpass filter (a) prototype passive structure (b) utilizing the L-C simulator in Figure 3.

The simulated frequency response of the implemented active bandpass filter is demonstrated in Figure 12 with the following components: $R = 1.5$ kΩ, $g_m = g_{m1} = g_{m2} = 0.675$ mA/V ($I_B = I_{B1} = I_{B2} = 100$ μA), and $C_A = C_B = 100$ pF. With $L_{eq} = 0.22$ mH and $C_{eq} = 100$ pF, the filter is designed to obtain $f_o = \omega_o/2\pi = 1.07$ MHz and $Q = 1$. The resulting responses demonstrate that the circuit can operate correctly between 500 kHz and 100 MHz.

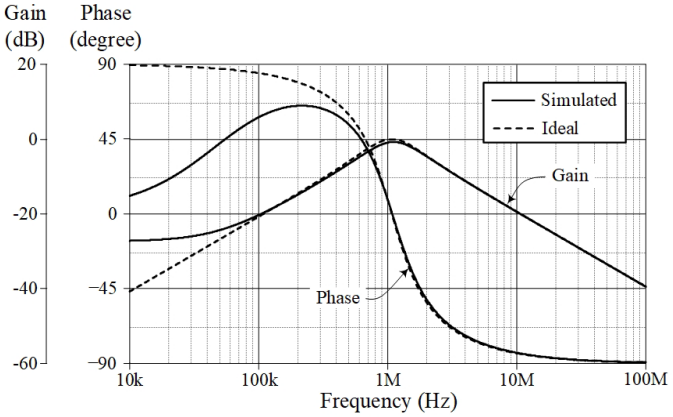


Figure 12: Ideal and simulated results of the bandpass frequency responses in Figure 11(b).

7. Conclusions

A grounded parallel RL, RC, and LC impedance simulator has been designed with VDBAs and two grounded passive components. Through the use of the transconductance parameter in VDBA, the simulated equivalent values, i.e., R_{eq}, L_{eq}, and C_{eq}, can all be electronically altered. The circuit has been simulated using the PSPICE program, which is based on 0.18-µm CMOS technology, to demonstrate its viability. In-depth laboratory tests have also been conducted to verify the practical usability of the simulator circuit. The design of a second-order voltage-mode bandpass filter using the proposed simulator is given.

Conflict of Interest

The authors declare no conflict of interest.

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