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Signal-to-Quantization Noise Ratio of the Parallel Digital Ramp Analog-to-Digital Converter

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ABSTRACT

This work presents a theoretical analysis of the Signal-to-Quantization Noise Ratio (SQNR) of the nonuniform Parallel Digital Ramp Pulse Position Modulator Analog-to-Digital Converter (PDR-ADC) architecture. The PDR-ADC partitions the amplitude axis into P non-overlapping partitions that sample the analog input at input signal driven instances. Samples are generated when the input signal crosses a digital ramp in a partition. The parallel digital ramps operate from a single clock. For sinusoidal signals, it is shown, for uniform partitions the SQNR can be increased be increasing the number of bits in the counter or by increasing the number of partitions. A geometric partitioning scheme is then proposed where, again for sinusoids, it is shown that this quantization rule has the effect of attempting to maintain the SQNR approximately constant. For geometric partitioning, it is shown that the largest SQNR is achieved when the geometric parameter, common ratio, equals two.

1 Introduction

Many alternatives to Nyquist rate sampling systems have been proposed in the literature [1] - [8]. Of the various methods described, the nonuniform Level Crossing (LC) architectures appear to dominate the recent literature, [9] -[14]. In [15], the PDR-ADC was introduced and circuits to affect the desired response developed. A specific partitioning scheme based upon partitioning the signal amplitude axis as a geometric series was developed in terms of circuit parameters. In this communication, alternative methods to increase the SQNR of the PDR-ADC and a more general discussion of the geometric partitioning in terms of the geometric progression parameter, common ratio, are presented.

All uniform quantizers begin to lose resolution as the amplitude of the input signal decrease. To understand where information is lost in uniform quantizers, a brief review of uniform quantization is presented. Next, the SQNR of the PDR-ADC is obtained under the conditions of a uniform partitioning scheme. The SQNR for a geometric partitioning scheme with common ratio two is developed without regard to any specific circuit analysis. Lastly, the SQNR for arbitrary common ratio is presented, where is is shown that the maximum increase in SQNR for geometric partitioning is obtained for a common ratio equal to two.

2 Uniform Quantization

Figure 1 is a block diagram of an ideal, uniform, analog to digital converter. The switch represents an ideal sample and hold (S&H) operation (aperture effects are ignored), such that the output of the S&H is the 'instantaneous' analog value of the input, $f(t)$. The quantization rule is represented by the Q block. Lastly, the encoder, E, converts the quantizer output into the corresponding digital word.

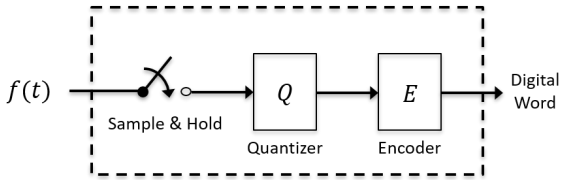

Figure 1: Ideal ADC

Let the number of bits in the digital word be, N, and let, V_{ref}, be the analog reference voltage for the ADC, then, as is well known, that the quantization step size, Δ is [15, 16]:

$$\begin{aligned} \Delta &= \frac{V_{ref}}{2^N} \\ &= \frac{V_{FS}}{2^N - 1} \end{aligned} \tag{1}$$

where V_{FS} is the *full scale* voltage: $V_{FS} = V_{ref} - \Delta$.

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In uniform quantizers, the quantization noise power, P_{N_Q}, is well approximated by, [17, 18]:

$$P_{N_Q} = \frac{\Delta^2}{12} \tag{2}$$

The signal-to-quantization noise ratio (SQNR) is the ratio of the signal power, P_{sig}, to the quantization noise power, P_{N_Q}. For a full scale sinusoid of the form, $y = \frac{V_{FS}}{2} sin(\omega t)$, the $SQNR$ is found to be:

$$\begin{aligned} SQNR = \frac{P_{sig}}{P_{N_Q}} &= \frac{(V_{FS}/2)^2}{2} \cdot \frac{12}{\Delta^2} \\ &\approx 2^{2N} \cdot \frac{3}{2} \end{aligned} \tag{3}$$

or in decibels, the familiar "rule of thumb" for sinusoids is obtained:

$$SQNR_{dB} \approx 6.02N + 1.76\ dB \tag{4}$$

Lastly, as is well known, when the amplitude of a sinusoidal signal decreases by a factor of 2, the signal power decreases by a factor of 4 and the ADC loses 1 bit of resolution. The $SQNR_{dB}$, from 4, may be written as:

$$SQNR_{dB} \approx 6.02(N-1) + 1.76\ dB \tag{5}$$

3 PDR: Uniform Partitions

Conceptually, the PDR-ADC may initially be regarded as a parallel arrangement of uniform quantizers as shown in Figure 2. Each quantizer, in Figure 2, is referenced independently and spans a different range of possible input signal values, thus partitioning the input signal axis [19, 15].

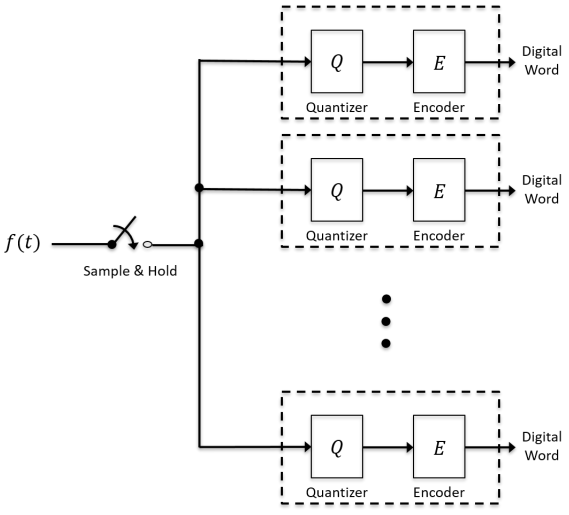

Figure 2: Parallel Quantization

In such an arrangement, if $\mathcal{P}$ is the number of partitions, and if each quantizer contains the same number of quantization levels, L, where $L = 2^N$, and if each quantizer has a dynamic range, $\frac{V_{ref}}{\mathcal{P}}$, so that together the $\mathcal{P}$ partitions span V_{ref}, then the quantization step size is given by:

$$\Delta = \frac{V_{ref}}{\mathcal{P} \cdot 2^N} \tag{6}$$

Such a parallel uniform partitioning scheme is illustrated in Figure 3 for a system with 4 partitions with 4 levels per partition.

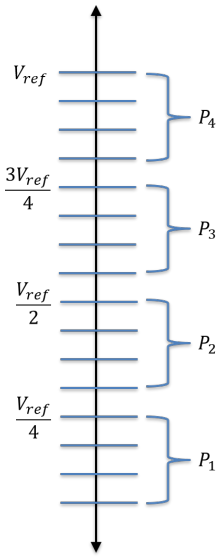

Figure 3: Parallel Uniform Partitioning

Equation (6) yields the same quantization step size as a single ADC with $L = \mathcal{P} \cdot 2^N$ levels, operating from the same V_{ref}.

The PDR-ADC, however, operates from a single N bit digital counter, that generates 2^N counts, that are scaled and shifted to generate the required number of partitions [15]. Consequently, if a single digital ramp ADC, operating with clock rate, T_{CLK}, were required to span the same dynamic range, V_{ref}, this single digital ramp would take $\mathcal{P} \cdot 2^N \cdot T_{CLK}$ seconds. The PDR-ADC however, spans the same dynamic range in $2^N \cdot T_{CLK}$ seconds, a $\frac{1}{\mathcal{P}}$ times improvement.

For a PDR-ADC, governed by (6), excited by a full scale sinusoid of the form, $y = \frac{V_{FS}}{2} sin(\omega t)$, the $SQNR$ is found to be:

$$SQNR \approx \mathcal{P} \cdot 2^N \cdot \frac{3}{2} \tag{7}$$

or in decibels:

$$SQNR_{dB} \approx 6.02N + 1.76 + 20log_{10}(\mathcal{P}) \tag{8}$$

Equation (8) states, in the PDR-ADC, with each partition operating with the identical, uniform, step size, Δ, the signal-to-quantization noise may be increased in the usual way by increasing the number of bits used in the counter, N, and/or by increasing the number of partitions, $\mathcal{P}$.

For example, the identical $SQNR$ performance of a single, 16 bit ADC can be achieved with a PDR-ADC designed with, $\mathcal{P} = 8$ partitions, operating with a 13 bit counter. Additionally, in this case, the PDR only counts to 8192, whereas a single digital ramp ADC would be required to count the full 65536 counts.

Additionally, in the PDR-ADC, the counter is not required to count, to a count value that is a power of 2. The same performance as described can be matched,

approximately, from a PDR-ADC designed with $\mathcal{P} = 10$ partitions and a counter that counts to 6554, thereby further decreasing the total time required to span the full dynamic range. A practical design constraint is that the number of partitions be even, so that the dynamic range of the PDR-DAC is symmetric about zero Volts.

4 PDR: Geometric Partitioning

In this section, the general behavior of the PDR-ADC with a geometric partitioning scheme of the amplitude axis, as illustrated in Figure 4, is presented without reference to circuit analysis[1]. For clarity, Figure 4 shows the essence of the geometric partitioning with a system of 4 partitions with 4 levels per partition. In the figure, the reference voltage of the entire system is equated to the maximum of the geometric sum, which is designated, $15V_x$, for the yet to be determined voltage, V_x.

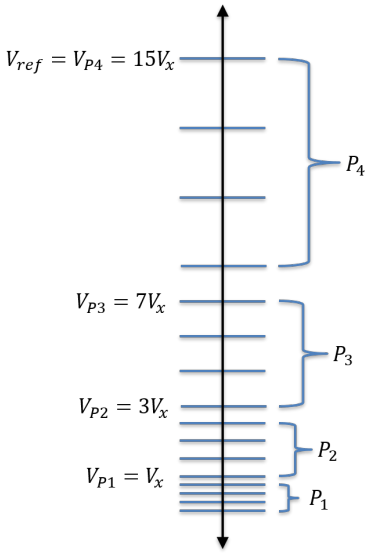

Figure 4: Parallel Geometric Partitioning

The m^{th} reference voltage, V_{P_m} for each partition is related as a geometric series, and is obtained from:

$$V_{P_m} = V_x \sum_{k=0}^{k=m-1} 2^k \tag{9}$$

Let $\mathcal{M}$ to be the maximum partition number, then, from the system reference voltage, V_{ref}, the voltage V_x may be found from:

$$V_{ref} = V_x \sum_{k=0}^{k=\mathcal{M}-1} 2^k = V_x\left(2^{\mathcal{M}} - 1\right) \tag{10}$$

from which:

$$V_x = \frac{V_{ref}}{2^{\mathcal{M}} - 1} \tag{11}$$

The ratio of the n^{th} term of a geometric progression to the $n^{th} + 1$ term is, $\frac{1}{r}$, where r is the common ratio, as is well known. If the common ratio is, $r = 2$, then as the number of partitions increases, the second to last partition is referenced to a value that *approaches* $\frac{V_{ref}}{2}$. In the case under consideration, the $\mathcal{M} - 1$ partition is referenced from:

$$\begin{aligned} V_{P_{\mathcal{M}-1}} &= \frac{V_{ref}}{2}\left(1 - \frac{1}{2^{\mathcal{M}} - 1}\right) \\ &\approx \frac{V_{ref}}{2} \end{aligned} \tag{12}$$

4.1 Geometric SQNR

In the PDR-ADC, for any adjacent partitions, the ratio of the quantization step sizes is the common ratio, which may be written as:

$$\frac{\Delta_m}{\Delta_{m+1}} = \frac{1}{2} \tag{13}$$

where this behavior can be seen in Figure 4.

From (2) and (13), it is seen, in the PDR-ADC, with common ratio, $r = 2$, the quantization noise power of adjacent partitions may be written as:

$$P_{N_{Qm}} = \frac{P_{N_{Qm+1}}}{4} \tag{14}$$

In a PDR-ADC, with geometric partitioning, the quantization noise power decreases by a factor of 4 when transitioning from a higher partition to a lower partition.

Let a full scale sinusoid of the for, $y = A_o sin(\omega t)$, be input to the PDR-ADC, the SQNR is of the form:

$$SQNR = \frac{P_{sig}}{P_{N_{Q\mathcal{M}}}} = \frac{A_o^2}{2} \cdot \frac{1}{P_{N_{Q\mathcal{M}}}} \tag{15}$$

Now, suppose the input signal amplitude decreases by a factor of 2 and let $y = \frac{A_o}{2} sin(\omega t)$ be input to the PDR-ADC, the SQNR is given by:

$$SQNR = \frac{1}{4} \cdot \frac{A_o^2}{2} \cdot \frac{1}{P_{N_{Q\mathcal{M}-1}}} \tag{16}$$

substituting (14) into (16) the SQNR is:

$$\begin{aligned} SQNR &= \frac{1}{4} \cdot \frac{A^2}{2} \cdot \frac{1}{P_{N_{Q\mathcal{M}}}/4} \\ &= \frac{A_o^2}{2} \cdot \frac{1}{P_{N_{Q\mathcal{M}}}} \end{aligned} \tag{17}$$

Equation (17) states, in the PDR-ADC, with a geometric partitioning, the signal-to-quantization noise attempts to remain approximately constant.

4.2 Constant SQNR

The constant value that the SQNR attempts to maintain can be obtained in terms of uniform ADC parameters with the aid of Figure 5. Figure 5 shows, on the left hand side, the uniform levels and the quantization step size for an 4 bit (16 Levels) uniform ADC with dynamic range, V_{FS}. The right hand side of Figure 5 shows the geometric partitioning for the same dynamic range. In the detail of Figure 5, the quantization step size of the largest partition is shown for a 4 bit counter that produces the same number of quatization

[1] A circuit realization of the geometric behavior can be found in [15].

levels (16 Levels) as the uniform quantizer shown on the left.

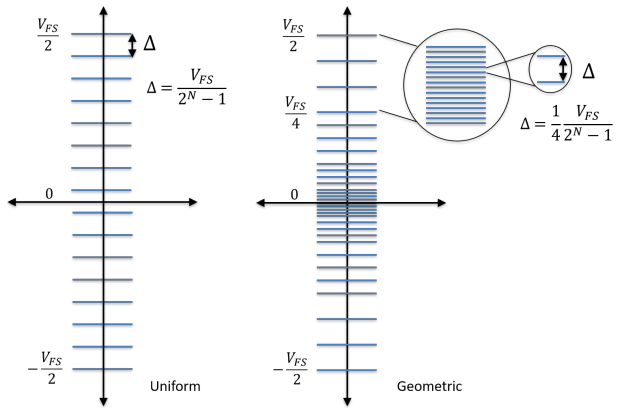

Figure 5: Constant Quantization Step Size

From (12), the dynamic range of the largest partition always approaches $\frac{1}{2}$ of the maximum voltage value, assuming a sufficient number of partitions. In the present case under consideration, as seen in Figure 5, this dynamic range is, $\frac{V_{FS}}{4}$. Consequently, when this range is divided by 2^N levels, the largest quantization step size of a PDR-ADC with geometric partitioning is:

$$\begin{aligned} \Delta_{max} &= \frac{1}{4}\frac{V_{FS}}{2^N - 1} \\ &= \frac{V_{FS}}{2^{(N+2)} - 4} \end{aligned} \tag{18}$$

Substituting (18) into (3), again assuming a full scale sinusoid of the form, $y = \frac{V_{FS}}{2} sin(\omega t)$, the SQNR is:

$$\begin{aligned} SQNR = \frac{P_{sig}}{P_{N_Q}} &= \frac{(V_{FS}/2)^2}{2} \cdot \frac{12}{\Delta_{max}^2} \\ &= \frac{12}{8} \cdot (V_{FS})^2 \cdot \frac{(2^{N+2} - 4)^2}{(V_{FS})^2} \\ &\approx \frac{3}{2} \cdot 2^{2(N+2)} \end{aligned} \tag{19}$$

or in decibels:

$$SQNR \approx 6.02\,(N + 2) + 1.76\ dB \tag{20}$$

Equation (20) states, for a full scale sinusoidal input, a PDR-ADC with geometric partitioning, operating from an N bit counter, gains 2 bits or resolution.

When the results of (20), (14) and (5) are taken together, for a PDR-ADC with geometric partitioning, operating from an N bit counter, the following behavior is deduced:

- From (20): The PDR-ADC behaves as a system with $N+2$ bits.
- From (5): When the signal amplitude drops by a factor of 2, the signal power drops by a factor of 4 and the system loses 1 bit of resolution.
- From (14): When the signal amplitude drops by a factor of 2, the quantization noise power drops by a factor of 4, and the system gains 1 bit of resolution, and the system continues to behave as a system with $N + 2$ bits of resolution.

With geometric partitioning, the PDR data converter attempts to maintain the signal-to-quantization noise ratio approximately constant.

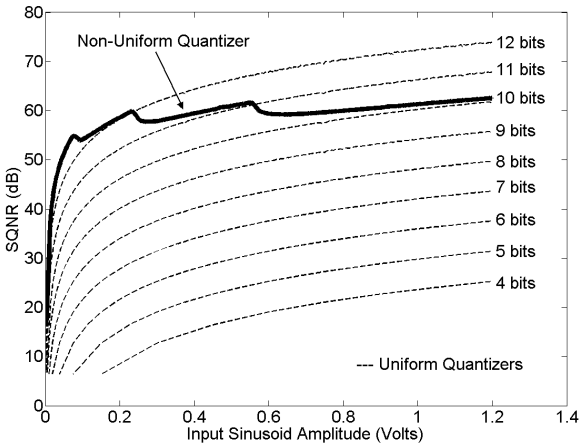

Figure 6: Approximately Constant SQNR from Geometric Partitioning

In Figure 6, the SQNR for the geometric partitioning, with common ratio $r = 2$, is shown as a function of input signal amplitude. The full scale voltage was, $V_{FS} = 2.4$ Volts and the system was driven with a sinusoid of the form, $y = A_o sin(\omega t)$, where A_o was varied from 1.2 Volts to approximately $1mV$. The PDR was modeled with $\mathcal{P} = 8$ partitions with an $N = 8$ bit counter.

For reference comparison, the SQNR for several uniform quantizers are also plotted in Figure 6. It is seen that the system performance is approximately equivalent to a system with $N = 10$ bits of resolution and that the system attempts to maintain this performance against variations in the peak signal amplitude. The peaking in the non-uniform quantizer are the locations where input signal voltage amplitude transitions from one partition to the adjacent partition.

5 Common Ratio and SQNR

Let the maximum voltage of the data converter be, $\frac{V_{FS}}{2}$, then, for any value of the common ratio, r, the maximum value of the next lower partition always approaches, $\frac{V_{FS}}{2r}$, using a geometric partitioning scheme. Consequently, the dynamic range of the largest (outer) partition, $\mathcal{M}$, is approximately:

$$\begin{aligned} \Delta V_{\mathcal{M}} &\approx \frac{V_{FS}}{2} - \frac{V_{FS}}{2r} \\ &= \frac{V_{FS}}{2} \cdot \left(\frac{r-1}{r}\right) \end{aligned} \tag{21}$$

Assuming that this voltage is spanned by an N bit counter, and if driven by a sinusoid, the SQNR becomes:

$$\begin{aligned} SQNR = &= \frac{(V_{FS}/2)^2}{2} \cdot \frac{12}{\Delta^2} \\ &= \frac{12}{8} \cdot (V_{FS})^2 \cdot \left(\frac{2r}{r-1}\right)^2 \cdot \frac{(2^N-1)^2}{(V_{ref})^2} \\ &= \frac{3}{2} \cdot \left(\frac{2r}{r-1}\right)^2 (2^N-1)^2 \\ &\approx \frac{3}{2} \cdot \left(2^{N+b}\right)^2 \end{aligned} \tag{22}$$

where $b = \frac{ln(\frac{2r}{r-1})}{ln(2)}$. Or in decibels:

$$SQNR \approx 6.02\,(N+b) + 1.76\,dB \tag{23}$$

In 23, as the common ratio, $r \to \infty$, $b \to 1$, and the system only gains 1 bit of resolution. Alternatively, as $r \to 2$, its minimum possible value, $b \to 2$, and the system gains 2 bits of resolution. It is seen, in the PDR with geometric partitioning, the largest increase in the effective number of bits occurs with the common ratio, $r = 2$.

6 Conclusion

The signal-to-quantization noise (SQNR) of the parallel digital ramp analog to digital (PDR-ADC) has been formulated using a more general analysis using the common ratio of a geometric series. It was shown that for all values of the common ratio, using a geometric partitioning scheme, the maximum possible increase in the SQNR is achieved when the common ratio, $r = 2$, and the effective increase in the number of bits of resolution provided by an N bit counter is accordingly, 2. It was shown that with geometric partitioning, the PDR-ADC attempts to maintain the SQNR approximately constant. Additionally, it was shown, using a uniform partitioning scheme provides more flexibility in the effective increase in the counters effective resolution with a trade off in the number of partitions, though in this case, the SQNR does not remain approximately constant.

Conflict of Interest The author declares no conflict of interest.

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