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A Novel Pulse Position Modulator for Compressive Data Acquisition

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ABSTRACT

This work extends the development of the nonuniform Parallel Digital Ramp Pulse Position Modulation Analog-to-Digital Converter (PDR-ADC) architecture. The continuous to discrete transform of the PDR-ADC is achieved by partitioning the signal amplitude axis into P nonoverlapping partitions that sample the analog input at input signal driven instances. Each partition contains L uniform levels with different quantization step sizes such that the dynamic range of the partitions are related as a geometric series. It is shown that this new architecture satisfies the Nyquist requirement on average (Beutler's condition) and results in a random additive sampling architecture that is alias free (Shapiro-Silverman condition). Additionally, it is shown that the geometric partitioning causes the signal-to-quantization noise ratio (SQNR) to remain approximately constant. A comprehensive design paradigm is presented, including circuits to affect the desired response, the format of the encoded digital samples and the corresponding transformation to determine the equivalent analog voltage. Lastly, although the thrust of this paper is not reconstruction techniques, reconstruction is, nevertheless, compulsory, and recovery and reconstruction is demonstrated through simulations.

1 Introduction

This communication is an extension of work originally presented at a conference on Electrical and Computer Engineering [1] and this current paper significantly expands upon the initial concept proposed in the original material. Although the most common form of sampling is uniform sampling, there are many cases where nonuniform sampling arises and is intentional [2]. Compressed Sensing (CS) ,[3, 4], is based upon, and operates on nonuniform samples. In CS, the goal is to compress at the time of sampling [5]. To combine acquisition and compression into one step necessitates new hardware innovations. The data converter proposed is a novel approach to nonuniform data acquisition.

The mathematical theory of nonuniform sampling and reconstruction has been well studied [6], and several hardware realizations have been described. In [7], the concept of the Level Crossing (LC) detector for nonuniform sampling was described and developed, in [8], the LC concept was extended and [9], an LC hardware design in 120nm CMOS was fabricated. In [10], the LC concept was extended to include a triangular dither signal on the input. In [11], the LC sampling scheme was used in an event driven ADC application for electrocardiogram (ECG) signal acquisition. In [12], an adaptive LC sampling scheme was developed, whereby the levels are no longer static but rather adapt to the required signal dynamic range. In [13], a time based ADC was proposed using pulse position modulation (PPM). In [14], a nonuniform sampling system based upon PPM using a reference ramp rest was proposed. In [15], a wideband nonuniform sampling system using a random modulator pre-integrator, similar to direct sequence spread spectrum, was described, and in [16] a nonuniform sampling system based upon pseudo-randomly (PN) triggering the sample-and-hold circuit in an otherwise standard ADC was proposed.

The new nonuniform architecture presented here is based on a parallel implementation of the standard Digital Ramp Pulse Position Modulators (PDR-ADC). The architecture partitions the amplitude range into $\mathcal{P}$ nonoverlapping partitions, each governed by its own digital ramp. The ensemble of digital ramps operate from a single counter N bit counter and a single Digital-

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to-Analog (DAC) converter, greatly simplifying the synchronization and calibration process. It is shown that our approach exhibits effective compressed sensing performance (compression and acquisition at the same time) at greatly reduced complexity.

2 Conventional PPM

Conventional Pulse Position Modulation (PPM) generates one sample per period of a reference ramp [1]. In the PPM waveform generator circuit shown in Figure 1, $f(t)$ is the input analog signal to be sampled and $r(t)$ is a saw tooth reference waveform with period, T_{ramp}. The comparator is assumed to be referenced from a positive voltage supply, V_{CC}, and a negative supply voltage supply V_{EE}. Pulse Width Modulation (PWM) is an ouput signal and PPM is the output Pulse Position Modulation signal generated by the monostable multivibrator (one shot) circuit. When triggered, a one shot produces a single pulse of fixed, finite duration.

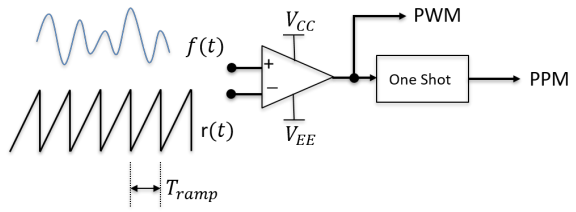


Figure 1: PPM Generator

A comparator, in general, will produce an output at the positive supply rail, V_{CC}, whenever the signal input to the noninverting amplifier terminal, $V_{\oplus}$, is greater than the signal input to the inverting amplifier terminal, $V_{\ominus}$. Similarly, the comparator output will be at the negative supply rail, V_{EE}, whenever $V_{\ominus} > V_{\oplus}$. For the circuit in Figure 1, the PWM output signal as a function of time may be expressed as:

$$PWM(t) = \begin{cases} V_{CC} & \text{if } f(t) > r(t) \\ V_{EE} & \text{otherwise} \end{cases} \tag{1}$$

Under the conditions specified, when $r(t)$ exceeds $f(t)$, the one shot will trigger and a sample generated. Assuming the bandwidth of the analog input, $f(t)$, is less than $\dfrac{1}{T_{ramp}}$, one sample is generated per period of the reference ramp and we may define the sample rate as, $FS = \dfrac{1}{T_{ramp}} \equiv \dfrac{1}{T_s}$.

Figure 2 is an illustration of several cycles of the reference ramp signal. In Figure 2, r_n is the n^{th} period of the reference signal. If we define the full scale voltage as, $V_{FS} = V_{CC} - V_{EE}$ and let the negative supply rail be such that, $V_{EE} = -V_{CC}$, as is typically the case, then we may write, $V_{FS} = 2V_{CC}$. We can then define the slope of the reference as, $\beta = \dfrac{V_{FS}}{T_s}$. By direct enumeration, $r_n(t)$ in Figure 2 is:

$$\begin{aligned} r_0(t) &= \beta t + V_{EE} && 0 \le t < t_1 \\ r_1(t) &= \beta t + V_{EE} - \beta t_1 && t_1 \le t < t_2 \\ r_2(t) &= \beta t + V_{EE} - \beta t_2 && t_2 \le t < t_3 \\ &\vdots \\ r_n(t) &= \beta t + V_{EE} - \beta t_n && nT_s \le t < (n+1)T_s \end{aligned} \tag{2}$$

Substituting $V_{EE} = -\dfrac{V_{FS}}{2}$, $V_{FS} = \beta T_s$ and $t_n = nT_s$, (2) becomes:

$$\begin{aligned} r_n(t) &= \beta t - \frac{\beta T_s}{2} - \beta n T_s \\ &= \beta t - \beta T_s\left(n + \frac{1}{2}\right) \qquad n = 0, 1, 2, \cdots \end{aligned} \tag{3}$$

The comparator triggers when $r(t) = f(t)$, from (3), the discrete sample time, τ_n, of the n^{th} pulse is:

$$\tau_n = nT_s + \frac{f_n}{\beta} + t_d \qquad n = 0, 1, 2, \cdots \tag{4}$$

where $\beta = \dfrac{V_{FS}}{T_s}$ and $t_d = \dfrac{T_s}{2}$.

Equation (4) shows, in conventional PPM not only is the timing of the n^{th} sample proportional to the sample number, n, the timing is also a function of the signal being sampled. Consequently, it is seen, conventional PPM generates nonuniform sampling.

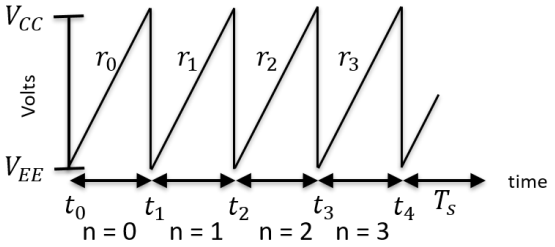


Figure 2: PPM Reference Ramp

3 Δ-PPM

It is possible to generate a PPM signal directly, without explicitly having the PWM output trigger a one-shot. Such a direct generation of the PPM signal is accomplished by resetting the reference ramp after the comparator triggers. Generating a PPM signal by resetting the reference ramp will be called, Δ–PPM, to distinguish it from conventional PPM. Δ–PPM may be generated with the circuit of Figure 3. In Figure 3, V_{CC} and V_{EE} are the power supplies for the comparator, $f(t)$ is the signal to be sampled and $r(t)$ is the reference ramp. Also shown in Figure 3 is a RESET circuit that asynchronously resets the reference ramp at each PPM pulse.

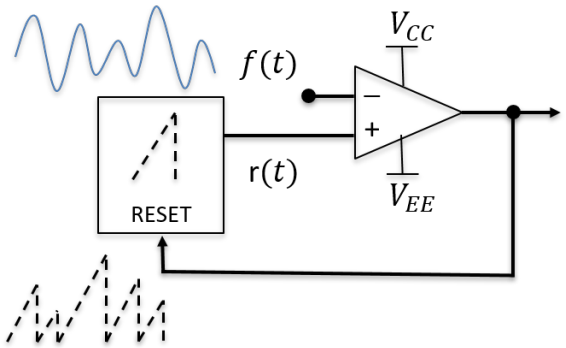


Figure 3: Reset PPM Generator

The previous periodicity of the reference signal is annihilated when the reference ramp is allowed to reset after the comparator triggers. An arbitrary response to the asynchronous triggering is shown in Figure 4. In Figure 4, we call r_n is the n^{th} response of the reference signal, rather than the n^{th} period of the reference, and again define the full scale voltage as, $V_{FS} = V_{CC} - V_{EE}$ and the slope of the reference as, $\beta = \dfrac{V_{FS}}{T_s}$.

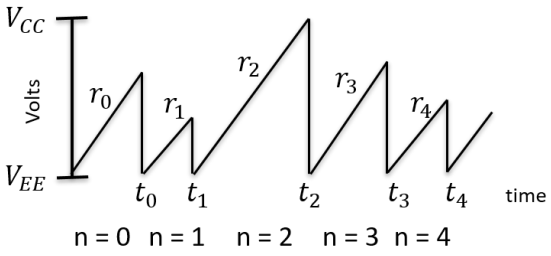


Figure 4: Reset PPM Reference Ramp

By direct enumeration, $r_n(t)$ in Figure 4 is:

$$\begin{aligned} r_0(t) &= \beta t + V_{EE} && 0 \le t < t_0 \\ r_1(t) &= \beta t + V_{EE} - \beta t_0 && t_0 \le t < t_1 \\ r_2(t) &= \beta t + V_{EE} - \beta t_1 && t_1 \le t < t_2 \\ &\vdots \\ r_n(t) &= \beta t + V_{EE} - \beta t_{n-1} && t_{n-1} \le t < t_n \end{aligned} \tag{5}$$

We note that the interval endpoints cannot be specified as constants, as was the case in conventional PPM, because they evolve dynamically. Again, substituting $V_{EE} = -\dfrac{V_{FS}}{2}$ with $V_{FS} = \beta T_s$, (5) becomes:

$$r_n(t) = \beta t - \beta t_{n-1} - \frac{\beta T_s}{2} \qquad t_{n-1} \le t < t_n \tag{6}$$

The comparator triggers when $r(t) = f(t)$, from (6), the discrete sample time, τ_n, of the n^{th} pulse is:

$$\tau_n = \tau_{n-1} + \frac{f_n}{\beta} + t_d \qquad n = 1, 2, 3, \cdots \tag{7}$$

where $\beta = \dfrac{V_{FS}}{T_s}$ and $t_d = \dfrac{T_s}{2}$.

Equation (7) shows, in Δ–PPM the timing of the n^{th} sample is a function of the signal being sampled and thus Δ–PPM generates nonuniform sampling, as in conventional PPM. Additionally, from (7), Δ–PPM samples times are a function of the previous sample time.

Two important consequence result if the sample times are a function of the previous sample time. First, Shapiro and Silverman [20] showed that sampling can be made alias free if each sample time is derived from the previous one by the addition of an independent random variable, from (7) it is seen that Δ–PPM provides such a sampling scheme. Second, Beutler [21] showed that if the sampling rate exceeds the Nyquist rate *on average* then the nonuniform sampling set will be stable and can be used to reconstruct a band-limited signal. We now show that Δ–PPM produces a sampling set with an average sampling rate,R_{avg}, that approaches, $R_{avg} = \dfrac{2}{T_s} \approx 2FS$.

Using (7) iteratively we may write:

$$\tau_n = \tau_o + n\frac{T_s}{2} + \frac{1}{\beta}\sum_{k=1}^{k=n} f_k \tag{8}$$

where τ_o is the first sampling instant.

Let $n \to N$, be the total number of samples such that $\{N : N \in 1, 2, 3, \ldots \infty\}$ and let τ_N be the maximum sample time, then, dividing by N:

$$\frac{\tau_N}{N} = \frac{\tau_o}{N} + \frac{T_s}{2} + \frac{1}{\beta}\left(\frac{1}{N}\sum_{k=1}^{k=N} f_k\right) \tag{9}$$

The last term in (9) is the average value of $f(t)$. If the average value equals zero, then the average sample rate is given by:

$$R_{avg} = \frac{2}{T_s}\left(\frac{N}{N + 2\tau_o/T_s}\right) \tag{10}$$

The maximum value of the first sampling instant is, $\tau_o = T_s$, which corresponds to the minimum value of R_{avg}, thus:

$$R_{avg} \ge \frac{2}{T_s}\left(\frac{N}{N+2}\right) \tag{11}$$

Less formally, for reasonable values of N experienced in practice, we may regard the average sample rate in Δ-PPM as, $R_{avg} = \dfrac{2}{T_s} \approx 2FS$.

The significance of (7) and (11) are that Δ–PPM is *self-regulating*. Δ–PPM automatically satisfies the Nyquist requirement on average (Beutler's condition [21]) and produces alias free random sampling (Shapiro-Silverman condition [20]). Additionally, Δ–PPM achieves self-regulation with no a priori knowledge of the signal support and does not utilize any particular code or special sequence to generate random samples.

4 Geometric Partitioning

The stylized, equal partitioning, presented [1], was intended to provide an introduction for the essence of the PDR-ADC. We now develop the elaboration of the partitioning scheme, where significant benefits will be obtained.

All data converters need an analog reference voltage to accomplish the continuous to discrete transform and produce a digital word [22]. In general, the converter divides an analog reference voltage, V_{REF}, into a fixed number of analog voltage levels, L. These analog voltage levels are then mapped to a digital number, typically referred to as counts. By convention, the smallest analog voltage level is assigned digital level $\boxed{0}$. The remaining analog voltage levels are mapped to digital levels by incrementing the ADC count. In this way, it is not possible to map the analog reference voltage, V_{REF}, to a number that can be reached and assigned a digital count.

All of the digital levels taken together define the scale. In general, there will be L levels and $L-1$ steps. The reference voltage divided by the number of levels defines the size of the analog step to reach an adjacent level. The step size, Δ, is sometimes referred to as the quantization step size or the least significant bit (LSB). The maximum analog voltage that can be mapped to a digital level is called the *full scale* voltage, V_{FS}. The relationship between the reference voltage, the full scale voltage and the quantization step size are shown in Figure 5 for a converter with $L = 16$ levels.

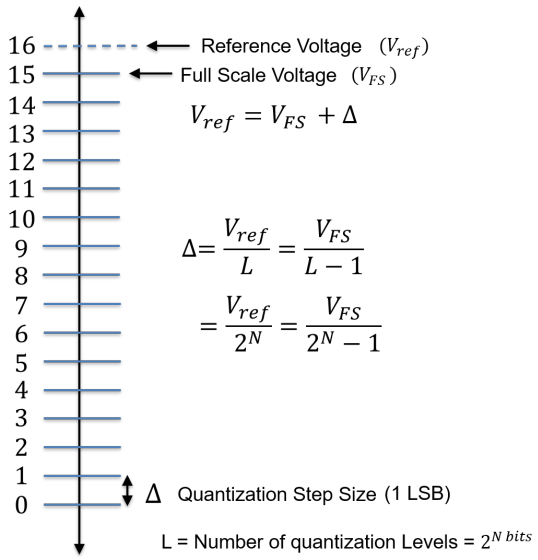


Figure 5: Quantization Step Size

The number of levels, L, is typically designed to be a function of the number of bits as, $L = 2^N$, where N is the number of bits. For the 4 bit converter shown in Figure 5, the reference voltage is divided by $16 = 2^4$. The first digital level is assigned digital count $\boxed{0}$, and corresponds to the digital number, $\boxed{0}\boxed{0}\boxed{0}\boxed{0}$. The maximum digital count is $\boxed{15}$, and corresponds to the digital number, $\boxed{1}\boxed{1}\boxed{1}\boxed{1}$. It is not possible to encode digital count $\boxed{16}$ with a 4 bit counter, and consequently, the reference voltage, V_{REF} in Figure 5, is not mapped to a digital number.

The principle of the geometric partitioning is shown in Figure 6 for a system with $\mathcal{P} = 8$ partitions and $L = 4$ levels. In the PDR data converter, the signal amplitude axis in partitioned into $\mathcal{P}$ partitions such that each partition contains L levels, the partitions do not overlap and each partition has a different quantization step size. The geometric partitioning is achieved by relating the spans (the dynamic range) of the partitions as a geometric series.

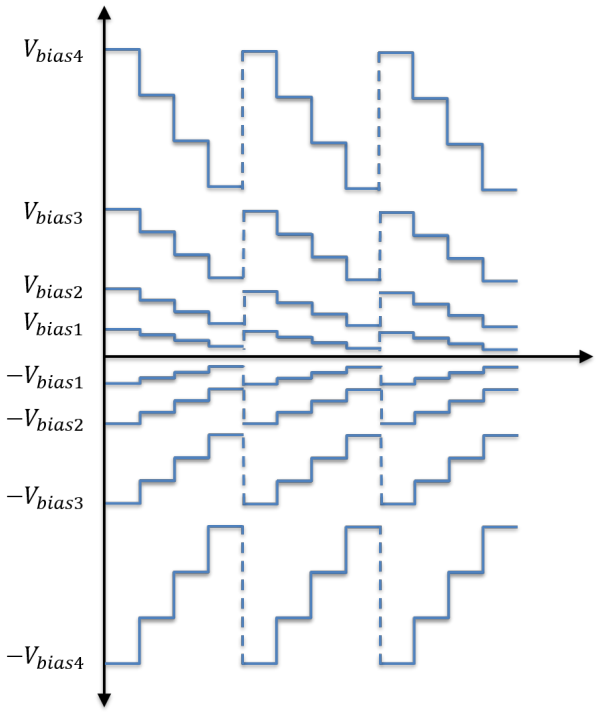


Figure 6: Geometric Partitioning: Conceptual

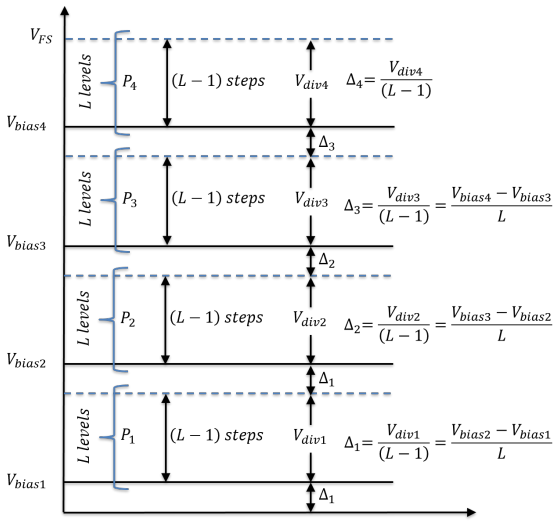


Figure 7: Geometric Partitioning: Detail

The relationship between partition bias voltages, V_{bias_m}, and the quantization step sizes needed to realize the behavior shown in Figure 6, can be better understood and visualized with the aid of Figure 7. Due to the symmetry of the bias voltages, only the positive partitions, P_1, P_2, P_3 and P_4, as shown in Figure 7, are needed.

Let the total number of partitions, $\mathcal{P}$, be even, and define the maximum partition number to be, $\mathcal{M} = \frac{\mathcal{P}}{2}$, and let m denote the m^{th} partition. In Figure 7, we denote by V_{div_m} the span of the m^{th} partition. By design, the spans of the partitions are geometrically related, thus:

$$\begin{aligned} V_{div2} &= 2V_{div1} = 2^{(2-1)}V_{div1} \\ V_{div3} &= 4V_{div1} = 2^{(3-1)}V_{div1} \\ V_{div4} &= 8V_{div1} = 2^{(4-1)}V_{div1} \\ &\vdots \\ V_{div_m} &= 2^{(m-1)}V_{div1} \quad m = 1, 2, 3, \cdots \mathcal{M} \end{aligned} \tag{12}$$

To realize (12), a circuit that takes the output from the DAC and applies the appropriate gain to compress the DAC steps is required. The required step compression response is shown in Figure 8 and the circuit to realize the response is shown in Figure 9.

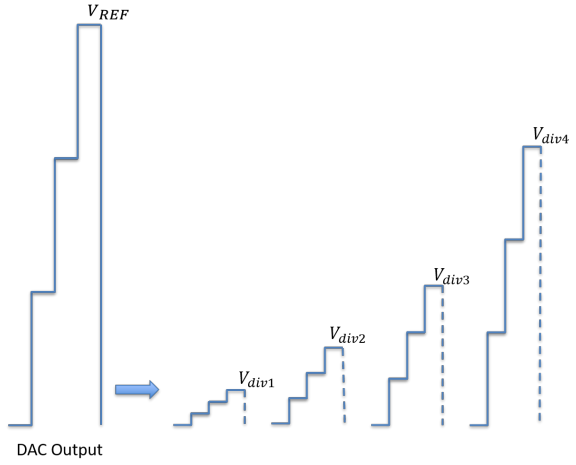


Figure 8: Step Compression Voltages

The step compression circuit in Figure 9 is a non-inverting voltage divider. To obtain design equations for the bias voltages in terms of the reference voltage, V_{REF}, the maximum number of partitions, $\mathcal{M}$ and the number of levels, L, we design the step compression circuit such that the voltage drop across resistor, $V_{Rx} = \left(2^{(\mathcal{M}-1)} - 1\right)V_{div1}$. Then, due to the geometric design and Kirchoff's voltage law, it must be the case:

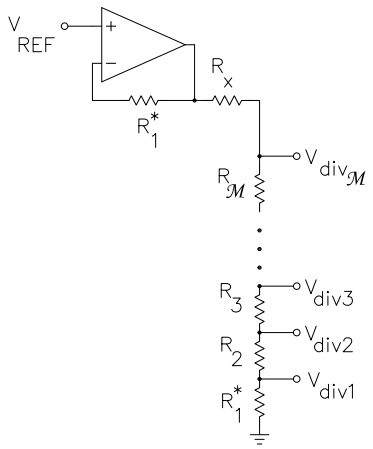


Figure 9: Step Compression Circuit

$$\begin{aligned} V_{REF} &= V_{div1} + V_{div2} + V_{div3} + \cdots + V_{div\mathcal{M}} \\ V_{REF} &= V_{div1}\left(1 + 2 + 4 + 8 + \cdots + 2^{(\mathcal{M}-1)}\right) \\ V_{REF} &= V_{div1}\sum_{k=0}^{k=\mathcal{M}-1} 2^k \\ V_{REF} &= V_{div1}\left(2^{\mathcal{M}} - 1\right) \\ &\therefore \\ V_{div1} &= \frac{V_{REF}}{2^{\mathcal{M}} - 1} \end{aligned} \tag{13}$$

From (12) and (13), the m^{th} voltage divider voltage is given by:

$$V_{div_m} = \left(\frac{2^{(m-1)}}{2^{\mathcal{M}} - 1}\right)V_{REF} \tag{14}$$

Dividing (14) by $L-1$, the quantization step size, Δ, is:

$$\Delta_m = \left(\frac{2^{(m-1)}}{2^{\mathcal{M}} - 1}\right)\left(\frac{V_{REF}}{L-1}\right) \tag{15}$$

Using Figure 7 and (14) and (15), we may write the bias voltages, V_{bias_m}, as:

$$\begin{aligned} V_{bias_m} &= \Delta_1 + \sum_{k=1}^{k=m-1}\left(V_{div_m} + \Delta_m\right) \\ V_{bias_m} &= \Delta_1 + \\ &\quad + \sum_{k=1}^{k=m-1}\left(\frac{2^{(m-1)}}{2^{\mathcal{M}} - 1}V_{REF} + \frac{2^{(m-1)}}{2^{\mathcal{M}} - 1}\frac{V_{REF}}{L-1}\right) \\ V_{bias_m} &= \Delta_1 + \frac{V_{REF}}{2^{\mathcal{M}} - 1}\left(\frac{L}{L-1}\right)\sum_{k=1}^{k=m-1} 2^{k-1} \\ V_{bias_m} &= \Delta_1 + \frac{V_{REF}}{2^{\mathcal{M}} - 1}\left(\frac{L}{L-1}\right)\left[2^{(m-1)} - 1\right] \\ V_{bias_m} &= \frac{V_{REF}}{2^{\mathcal{M}} - 1}\left(\frac{L}{L-1}\right)\left(2^{(m-1)} - 1 + \frac{1}{L}\right) \end{aligned} \tag{16}$$

Lastly, the Full Scale voltage shown in Figure 7 may be obtained by adding the results of (16) and (14) evaluating at $m = \mathcal{M}$:

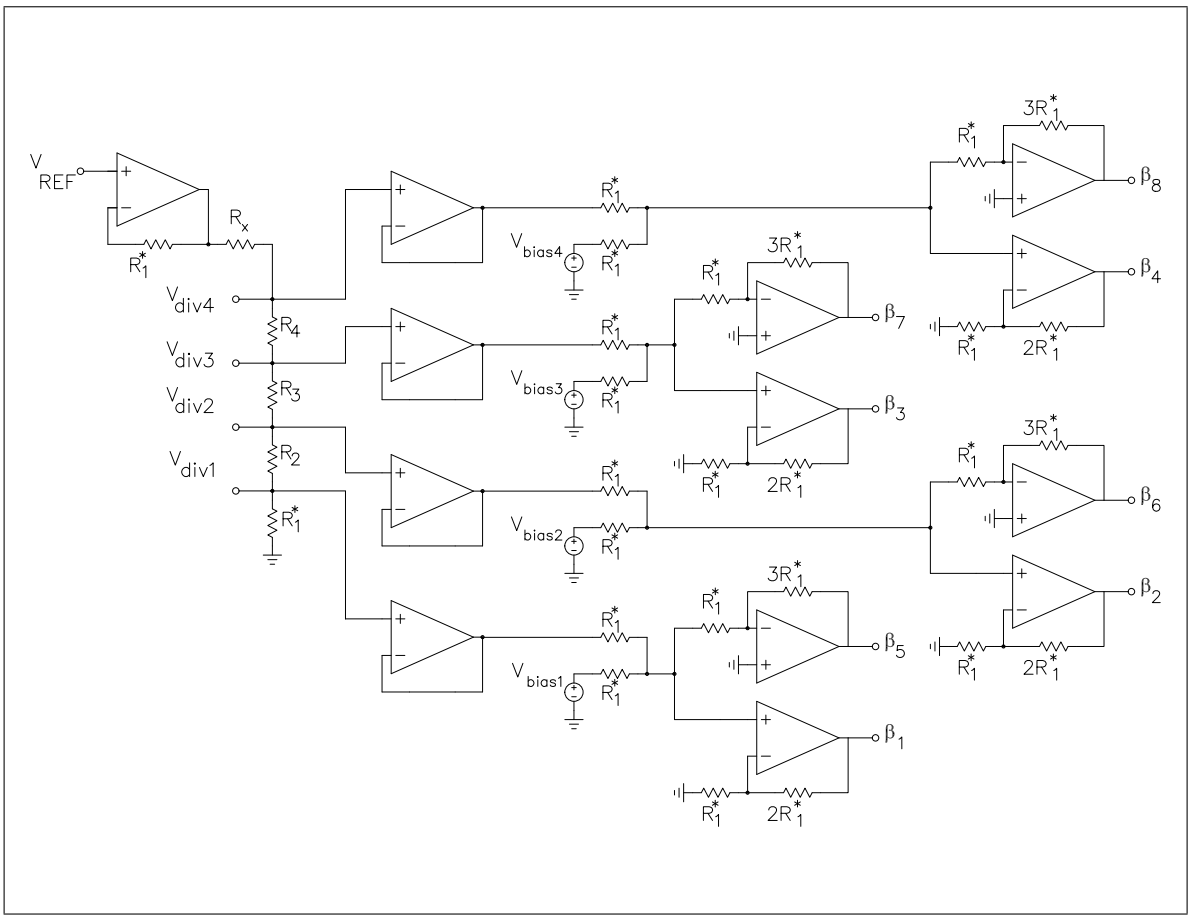


Figure 10: Step Compression & Level Shifting Circuit

$$V_{FS} = \frac{V_{REF}}{2^{\mathcal{M}}-1}\left(\frac{L}{L-1}\right)\left[2^{\mathcal{M}}-1+\frac{1-2^{(\mathcal{M}-1)}}{L}\right] \tag{17}$$

In terms of the external design parameters, V_{REF}, $\mathcal{M}$ and L, the number of partitions, $\mathcal{M}$ will have the most influence on the design equations, (16) and (17), since the bias is proportional to $\dfrac{1}{2^{\mathcal{M}}-1}$.

5 Step Compression and Level Shifting

We now develop the circuit to generate the parallel digital ramps shown in Figure 6, and we call this function, step compression and level shifting (SCLS). The step compression and level shifting circuit is shown in Figure 10. Step compression is governed by equations (14) and (15) and we seek now to determine design equations for the resistance for the circuit in Figure 10.

5.1 Step Compression

The step compression gains can be realized from circuit analysis by solving for the resistor values, in Figure 8, required to establish the voltage divider voltages, V_{div_m} as given by (14).

Let $\sum R_m = R_1^* + R_2 + R_3 + \cdots + R_{\mathcal{M}}$, then from circuit analysis:

$$V_{div1} = V_{REF}\left(\frac{R_1^*}{R_x + \sum R_m}\right) \tag{18a}$$

and in general:

$$V_{div_m} = V_{REF}\left(\frac{R_1^* + R_2 + R_3 + \cdots + R_m}{R_x + \sum R_m}\right) \tag{18b}$$

Divide (18b) by (18a):

$$\frac{V_{div_m}}{V_{div1}} = \frac{R_1^* + R_2 + R_3 + \cdots + R_m}{R_1^*} \tag{19}$$

Substituting the geometric relation given in (12) for V_{div_m}:

$$2^{(m-1)}R_1^* = R_1^* + R_2 + R_3 + \cdots + R_m = \sum R_m \tag{20a}$$

from which it is seen:

$$\begin{aligned} m = 2 &\longrightarrow R_2 = R_1^* \\ m = 3 &\longrightarrow R_3 = 2R_1^* \\ m = 4 &\longrightarrow R_4 = 4R_1^* \\ &\vdots \end{aligned} \tag{20b}$$

and in general:

$$R_m = 2^{(m-2)}R_1^* \quad \text{for} \quad m > 1 \tag{20c}$$

Lastly, from Equation (13) and (18a):

$$\frac{1}{2^{\mathcal{M}}-1} = \frac{R_1^*}{R_x + \sum R_{\mathcal{M}}} \qquad R_x = \left(2^{\mathcal{M}}-1\right)R_1^* - \sum R_{\mathcal{M}} \tag{21a}$$

and from (20a):

$$R_x = \left(2^{\mathcal{M}}-1\right)R_1^* - 2^{(\mathcal{M}-1)}R_1^* \qquad R_x = \left[2^{(\mathcal{M}-1)}-1\right]R_1^* \tag{21b}$$

To complete the design of the Step Compression circuit, we must specify a value for resistor R_1^*. To do so, we seek a design equation that relates the RMS noise voltage of the resistor to the voltage of the smallest quantization step size, Δ_1 in Figure 7. We then design the resistor value be *less* than this value so that the system is limited by the quantization noise of the LSB rather than the thermal noise of the resistor.

From (15):

$$\Delta_1 = \frac{V_{REF}}{(2^{\mathcal{M}}-1)(L-1)} \tag{22}$$

Assuming the noise is Gaussian distributed, then approximately all of the noise is contained within 6.6 standard deviations[1]. The peak-to-peak thermal noise voltage of the resistor is given by:

$$V_{pp\mathcal{N}_{th}}|_{R_1^*} = 6.6\sqrt{(4RkT\mathcal{B})} \tag{23}$$

where R is the resistance in Ohms, k is Boltzmann's constant ($k \approx 1.30865\times10^{-23}J/K$), T is the temperature in Kelvin and $\mathcal{B}$ is the bandwidth in Hertz.

To design for the thermal noise voltage of R_1^* to be less than Δ_1, we should select R_1^*, such that:

$$R_1^* \le \left(\frac{1}{6.6}\right)^2\left(\frac{V_{REF}}{(L-1)(2^{\mathcal{M}}-1)}\right)^2\left(\frac{1}{4kT\mathcal{B}}\right) \tag{24}$$

5.2 Level Shifting

Level shifting is governed by the bias voltages as given by (16). The aim of the level shifting circuit is to shift the step compressed voltages, shown in Figure 8, to the required bias level, shown in Figure 6. The β_m signals, in Figure 10, are the final step compressed and level shifted signals that are feed back to the input comparators [1]. From the symmetry of the design, the positive shifted β signals are given by:

$$\beta_m = V_{div_m} + V_{bias_m} \quad \text{for} \quad 1 \le m \le \mathcal{M} \tag{25}$$

and the negative shifted signals are given by:

$$\beta_{\mathcal{M}+m} = -\left(V_{div_m} + V_{bias_m}\right) \text{ for } 1 \le m \le \mathcal{M} \tag{26}$$

Specifically, for the β signals shown in Figure 10,:

$$\begin{aligned} \beta_1 &= V_{div1} + V_{bias1} & \beta_5 &= -(V_{div1} + V_{bias1}) \\ \beta_2 &= V_{div2} + V_{bias2} & \beta_6 &= -(V_{div2} + V_{bias2}) \\ \beta_3 &= V_{div3} + V_{bias3} & \beta_7 &= -(V_{div3} + V_{bias3}) \\ \beta_4 &= V_{div4} + V_{bias4} & \beta_8 &= -(V_{div4} + V_{bias4}) \end{aligned} \tag{27}$$

[1] 6σ is often used, however, 6.6σ is becoming an industry standard.

The design is readily obtained if the inverting and noninverting amplifiers in 10 are solved with the feedback resistors as arbitrary unknown resistors (2 degrees of freedom) and the remaining resistors fixed, equal to resistor R_1^*. A pair of inverting and noninverting amplifiers are shown in Figure 11 where $R_{\ominus}$, is the resistor in the inverting amplifier and $R_{\oplus}$ is the resistor in the non-inverting amplifier.

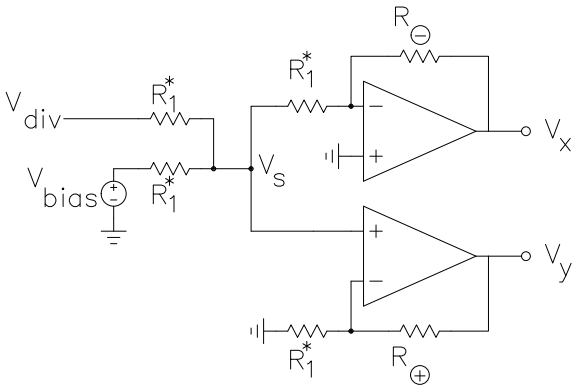


Figure 11: Level Shifting Feedback Scaling

From circuit analysis, the node voltage, V_s is:

$$\frac{V_s - V_{div}}{R_1^*} + \frac{V_s - V_{bias}}{R_1^*} + \frac{V_s}{R_1^*} = 0 \qquad V_s = \frac{V_{div} + V_{bias}}{3} \tag{28}$$

For the inverting amplifier we have, $\frac{V_s}{R_1^*} = -\frac{V_x}{R_{\ominus}}$, from which:

$$V_x = -\frac{R_{\ominus}}{R_1^*}\left(\frac{V_{div} + V_{bias}}{3}\right) \tag{29}$$

The required inverting sum, as given in (27), is obtained when:

$$R_{\ominus} = 3R_1^* \tag{30}$$

Similarly, for the non-inverting amplifier we have: $V_y = \left(1 + \frac{R_{\oplus}}{R_1^*}\right)V_s$, from which:

$$V_y = \left(1 + \frac{R_{\oplus}}{R_1^*}\right)\left(\frac{V_{div} + V_{bias}}{3}\right) \tag{31}$$

The required non-inverting sum, as given in (27), is obtained when:

$$R_{\oplus} = 2R_1^* \tag{32}$$

6 Maximum Sample Rate

Samples are generated by the precision windowed dual slope edge detector shown in Figure 12. The edge detector triggers an asynchronous LOAD flip-flop that stores the instantaneous value of the counter to memory. The LOAD signal, additionally, "sets" an RS flip-flop that drives the synchronous RESET flip-flop. On the next CLOCK, T_{clk}, the RESET flip-flop resets the counter. The counter generates a HOLD OFF signal that inhibits additional LOAD signals until the counter has settled, where the safety time to settle is 1 CLOCK pulse. The sampling circuit is shown in Figure 12.

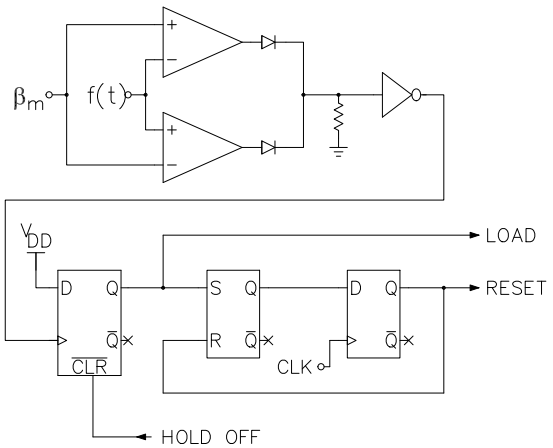


Figure 12: Windowed Synchronous One-Shot

In the PDR data converter, we must ensure that the counter has settled before the next LOAD/RESET cycle. The worst case signaling (fastest signal) corresponds if the LOAD signal aligns with a CLOCK edge. In such a case, a minimum of 3 CLOCKS is required to guarantee correct conversion before the next LOAD signal is allowed to register a new sample, this worst case timing is shown in Figure 13.

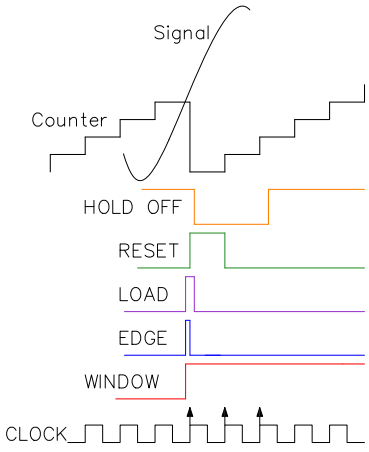


Figure 13: LOAD/RESET Timing

To determine the maximum signal frequency that the PDR-ADC can accommodate, we equate the maximum rate of change of the input signal, to the maximum rate of change allowable by the PDR. With an input sinusoid of the form, $f(t) = V_{FS} sin(2\pi f_{sig} t)$, the maximum rate of change is: $\frac{\Delta V}{\Delta t} = 2\pi f_{sig} V_{FS}$. The fastest rate of change the PDR can respond to is: $\frac{\Delta V}{\Delta t} = \frac{2V_{FS}}{3T_{clk}}$. The maximum signal frequency is:

$$f_{sig_{max}} = \frac{1}{3\pi T_{clk}} \tag{33}$$

7 The Counting Vector

In this section, we establish some important properties of the counting vector. Each intersection of $f(t)$ with a reference counter step contributes to the counting vector, $\boldsymbol{\alpha}$. The counting vector is responsible for determining the time of each sample, the amplitude of each sample, and the number of samples acquired. The counting vector also contains the information about the number of missing samples and where these missing samples are located. Information regarding the missing samples is critically important for reconstruction as the location and number of the missing samples (the data to be interpolated) must be known.

We denote by α, the number of counts accumulated by the counter. If the counter is strictly counting up, then the time to accumulate α counts, $t_\alpha = (\alpha + 1)T_{clk}$, where T_{clk} is the clock period. The time of the n^{th} sample, $t_{[n]}$, is the cumulative sum of the t_α's:

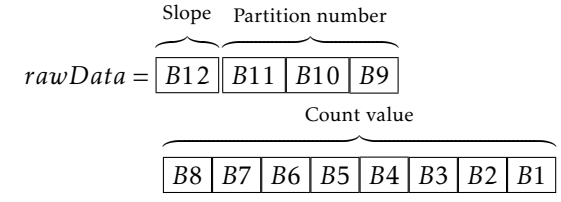
$$t_{[n]} = T_{clk} \sum_{i=1}^{i=n} (\alpha_i + 1) \tag{34}$$

If, instead, the counter is strictly counting down, we denote by α_c (the complement of α) the number of counts accumulated by the counter. In this way, $\alpha_c = (L-1) - \alpha$, where $L-1$ is the maximum value of the counter. In this case, the time of the n^{th} sample is:

$$t_{[n]} = T_{clk} \sum_{i=1}^{i=n} (L - \alpha_i) \tag{35}$$

The direction of the counter can be changed, by using a toggle flip-flop clocked on each RESET signal, and the system will continue to maintain the correct timing of each sample.

To recover the signal requires a method to resolve the counter slope, the partition number and the count value. We append, to the counting vector, additional bits that correspond to the counter slope and the partition number. As a specific example of accommodating partition encoding, suppose a PDR-ADC is designed with $\mathcal{P} = 8$ partitions and $L = 256$ levels per partition. The partition encoder requires 3 bits, the count slope requires 1 bit and the count value requires 8 bits, the data word stored in memory will be of the form:



In this example, the partition number in each data word is determined by:

$$m_i = rawData_i\ [B_{11} : B_9][\ 4\ 2\ 1\ ]^T \tag{36}$$

and each α_i is determined by:

$$\begin{aligned} \alpha_i &= rawData_i\ [B_8 : B_1]\mathbf{W}^T \\ &\equiv \mathbf{B}_i\mathbf{W}^T \end{aligned} \tag{37}$$

where, $\mathbf{W}$ = [128 64 32 16 8 4 2 1].

In general, once the i^{th} partition number, m_i, and the i^{th} count, α_i, have been determined, the sampled voltage value is given by:

$$V_i = \alpha_i \Delta_{m_i} + V_{bias_{mi}} \tag{38}$$

where Δ_m is given by (15) and V_{bias_m} is given by (16).

Lastly, since $\alpha_i + 1$ is the number of clocks to obtain α_i counts, then α_i is equal to the number of missing samples if the signal had been sampled at a rate equal to T_{clk}.

8 Signal to Quantization Noise Ratio (SQNR)

The signal to noise ratio (SNR) is always equal to the ratio of the signal power, P_{sig}, to the noise power, $P_{\mathcal{N}_Q}$. In data converters, the "noise" added by the system due to the act of approximating (truncating) a continuous function to finite precision is quantization noise, and the ratio of interest is the signal to quantization noise, $SQNR = P_{sig}/P_{\mathcal{N}_Q}$. In uniform quantizers, the quantization noise power is well approximated by, [17], [23]:

$$P_{\mathcal{N}_Q} = \frac{\Delta^2}{12} \tag{39}$$

In the PDR data converter, from (15), for any adjacent partitions:

$$\frac{\Delta_m}{\Delta_{m+1}} = \frac{1}{2} \tag{40}$$

from (39) and (40):

$$P_{\mathcal{N}_{Qm}} = \frac{P_{\mathcal{N}_{Qm+1}}}{4} \tag{41}$$

For the PDR, (41) states, the quantization noise power decreases by a factor of 4 when transitioning from a higher partition to a lower level partition. This effect is shown in the bottom panel in Figure 14, where, for comparison, we have also plotted the quantization error of a uniform quantizer in the top panel.

Let a signal of the form, $y = A_o sin(\omega_o t)$, be input to a uniform quantizer with quantization noise power, $P_{\mathcal{N}_{Qu}}$, the SQNR is given by:

$$SQNR_u = \frac{P_{sig}}{P_{\mathcal{N}_{Qu}}} = \frac{A_o^2}{2}\frac{1}{P_{\mathcal{N}_{Qu}}} \tag{42}$$

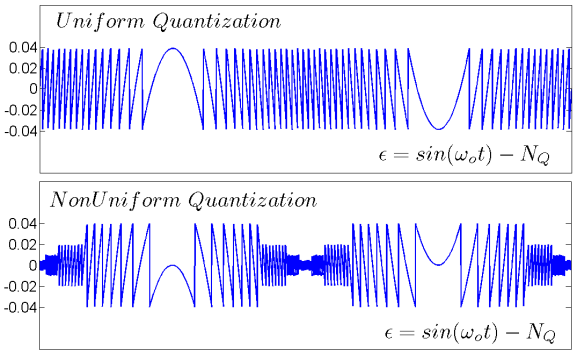


Figure 14: Quantization Error Comparison

Now suppose a signal of the form, $y = \frac{A_o}{2} sin(\omega_o t)$ is input to this uniform quantizer, the SQNR becomes:

$$SQNR_u = \left(\frac{1}{4}\right)\frac{A_o^2}{2}\frac{1}{P_{\mathcal{N}_{Qu}}} \tag{43}$$

From (42) and (43), in a uniform quantizer, when the input signal amplitude decreases by a factor of 2, the SQNR degrades by a factor of 4.

Now consider a signal of the form, $y = A_o sin(\omega_o t)$, input to the nonuniform PDR quantizer with quantization noise power, $P_{\mathcal{N}_{Qnu}}$, the SQNR is given by:

$$SQNR_{nu} = \frac{P_{sig}}{P_{\mathcal{N}_{Qnu}}} = \frac{A_o^2}{2}\frac{1}{P_{\mathcal{N}_{Qnu}}} \tag{44}$$

Again, suppose the input signal amplitude decreases by a factor of 2 and let $y = \frac{A_o}{2} sin(\omega_o t)$ be input to the nonuniform PDR quantizer, then, by (41), the SQNR becomes:

$$\begin{aligned} SQNR_{nu} &= \left(\frac{1}{4}\right)\frac{A_o^2}{2}\frac{1}{P_{\mathcal{N}_{Qnu}}/4} \\ &= \frac{A_o^2}{2}\frac{1}{P_{\mathcal{N}_{Qnu}}} \end{aligned} \tag{45}$$

From (44) and (45), it is seen, the geometric partitioning of the PDR-ADC attempts to maintain the signal-to-quantization noise ratio constant, this is a significant improvement compared to uniform quantization data converters.

We shall now be concerned with determining this constant. In an N bit uniform quantizer, the quantization step size, Δ_u, is:

$$\Delta_u = \frac{2V_{FS}}{2^N - 1} \tag{46}$$

Suppose we have a PDR data converter, with maximum partition number, $\mathcal{M}$, and $L = 2^N$ levels per partition, where N is the same as the uniform quantizer in (46). In the PDR, the largest quantization step size is given by (15), evaluated at $m = \mathcal{M}$.

$$\begin{aligned} \Delta_{\mathcal{M}} &= \left(\frac{2^{(M-1)}}{2^{\mathcal{M}} - 1}\right)\left(\frac{V_{REF}}{2^N - 1}\right) \\ &\approx \left(\frac{1}{2}\right)\left(\frac{V_{REF}}{2^N - 1}\right) \end{aligned} \tag{47}$$

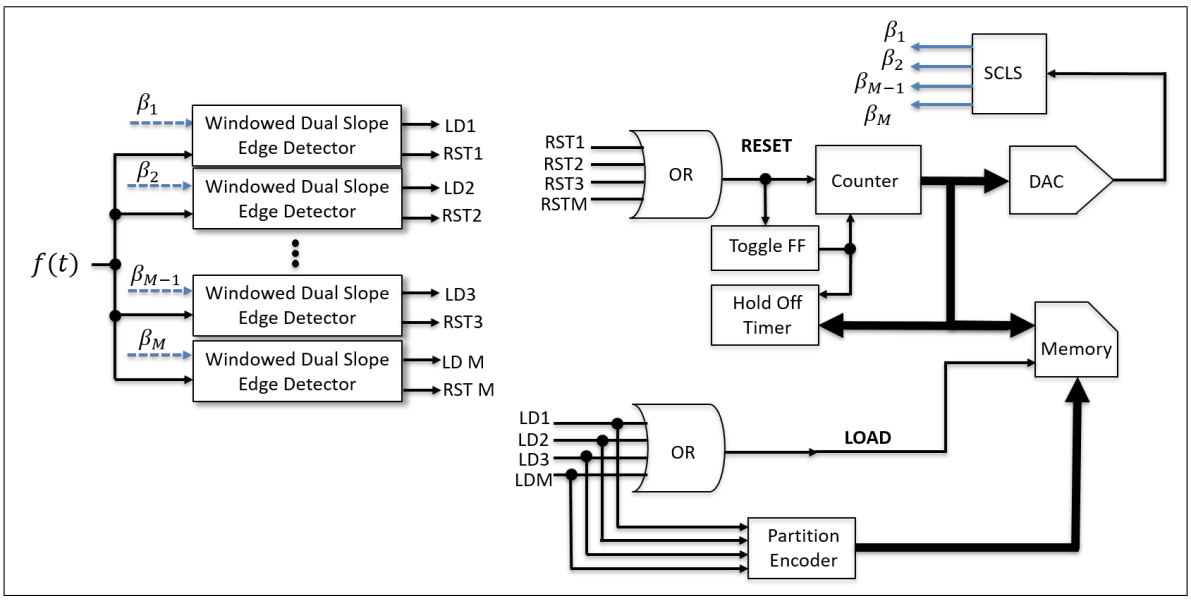


Figure 15: Parallel Digital Ramp ADC Overall Block Diagram

Using (46), we may write (47) as:

$$\Delta_{\mathcal{M}} \approx \left(\frac{1}{4}\right)\left(\frac{2V_{REF}}{2^N - 1}\right) = \frac{2V_{REF}}{2^{(N+2)} - 4} \tag{48}$$

In a PDR data converter, with $L = 2^N$ levels per partition, (48) states, the PDR has gained approximately 2 bits of resolution compared to a uniform quantizer.

The results of (45) and (48) may be summarized as, given a PDR data converter with $L = 2^N$ levels, the SQNR of the system will be approximately equivalent to a uniform system with $L = 2^{(N+2)}$ levels and the PDR will attempt to maintain this performance for all input signal levels.

9 Simulation Results

The proposed parallel digital ramp ADC was modeled and simulated in Simulink® and the reconstruction performed in Matlab®. The overall block diagram of the new ADC is shown Figure 15.

9.1 Linearity

The linearity of the PDR was analyzed empirically using a triangle wave, as shown in Figure 16, since, by design, the sampled data is not equally spaced. This approach was taken because the data converter figure of merit, Differential Non-Linearity (DNL), is a function of the difference of consecutive samples with a constant step size, as given by (49), where for an ideal ADC, the DNL = 0 [18]. In the PDR, since large gaps appear in the data and the step size is not constant, linearity is more easily performed graphically.

$$DNL[k] = \frac{ADC_{out}[k] - ADC_{out}[k-1]}{\Delta_{LSB}} - 1 \tag{49}$$

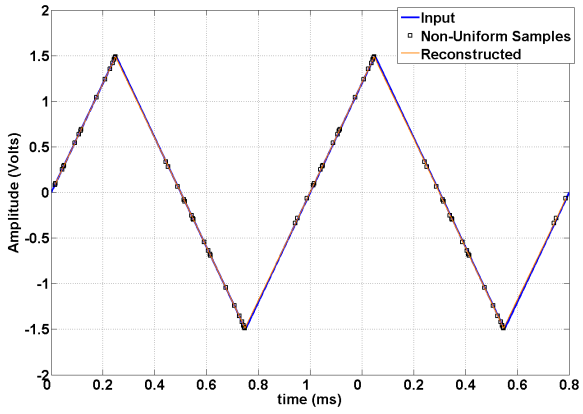


Figure 16: Reconstructed Linear

9.2 Electrocardiogram (ECG) Reconstruction

To test the new PDR data converter to acquire and reconstruct an analog signal from its nonuniform samples, a simulated electro-cardiogram (ECG) signal [25] was used. These signals have a wide dynamic range and "contain the QRS complex, which ensures oscillations near the Nyquist rate" [26] and are thus useful in exercising the nonuniform sampling architecture of the PDR.

The simulated ECG signal was modeled with a 1mV peak amplitude with 0.3mV DC offset and zero mean Gaussian noise with noise variance $\sigma_{\mathcal{N}o} \approx 0.058nW$ was added to the signal.

A wide view of the simulated run time of 10 seconds is shown in Figure 17, which demonstrates the PDR's ability to maintain the count. A zoom view of the reconstructed signal is shown in Figure 18, highlighting the features of the QRS pulse. When the signal is "idle" (DC like), and loiters near 0 Volts, the system continues to generate samples and is not adversely affected by the lack of signal dynamics.

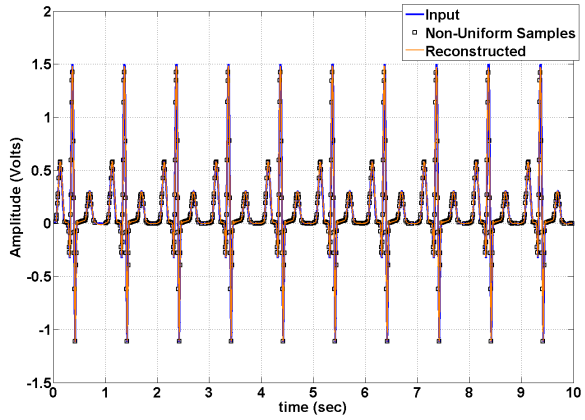


Figure 17: Reconstructed (simulated) ECG: Wide View

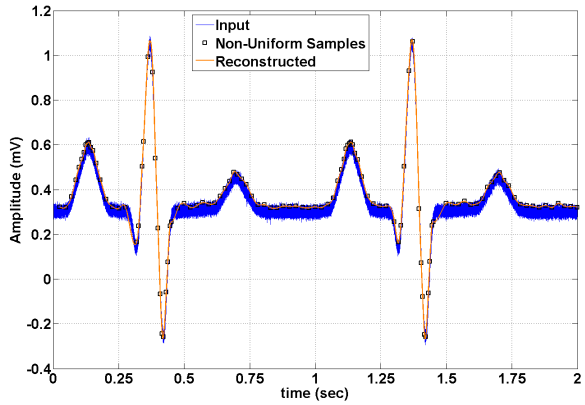


Figure 18: Reconstructed (simulated) Noisy ECG: Zoom View

10 Conclusion

A novel Analog-to-Digital Converter architecture based on partitioning the signal amplitude axis as a geometric series has been described. A detailed analysis of the design requirements to achieve the geometric partitioning has been provided and the essential circuits to realize the design presented. To extract the information content in each nonuniform digital sample, a proposed format of the nonuniform data was established, where it was shown that the partition number must be included in the digital word. Using reset Δ–PPM was shown to cause the system to satisfy the Nyquist requirement on average, and the geometric partitioning was shown to cause the SQNR to attempt to remain approximately constant. Lastly, the linearity of the PDR and the reconstruction of a simulated ECG signal were illustrated through simulation.

Conflict of Interest The authors declare no conflict of interest.

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