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A novel mixed-mode universal biquad employing plus current output DVCCs

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ABSTRACT

This paper refers to a novel mixed-mode universal biquad employing plus current output differential voltage current conveyors with grounded passive components. The circuit performs mixed-mode operation with the selection of the input and output terminals, and it enables low-pass, band-pass, high-pass, band-stop and all-pass responses choosing suitable input signals. The circuit needs no component matching constraints for obtaining five basic circuit responses above, and can adjust orthogonally the characteristic parameters by the circuit component. Additionally, the circuit has extremely low sensitivities with respect to the circuit components. A circuit design is performed with PSPICE simulation in order to verify the workability of the circuit.

1. Introduction

Active circuit with high performances (i.e. high frequency operation, low power dissipation, wide dynamic range, etc.) is receiving significant attention. Numerous circuit designs using some active devices such as operational trans-conductance amplifiers (OTAs), second generation current conveyors (CCIIs) and differential voltage current conveyors (DVCCs), etc. have been reported in the literature earlier [1-12].

A DVCC is a very useful active device, and DVCC-based circuit is adaptable to wideband operation. A plus current output DVCC (PO-DVCC) is composed of simpler circuit configuration than a minus current output one. Hence it has low power performance compared to the minus current output DVCC. Several voltage-mode (VM) and current-mode (CM) circuits have been synthesized by employing the DVCCs previously [8-11].

A biquad circuit is a typical second-order building block, and it is used for configuring various types of high-order circuits. It is required for circuit designers that the circuit enables some kinds of circuit responses without any component matching constraints, and that it has orthogonal or independent adjusting for characteristic parameters. Additionally, the circuit configuration employed grounded passive components is much recommended for CMOS implementation.

In actuality, active circuit may be claimed to operate in the mixed-modes (i.e. the VM, CM, trans-admittance-mode (TAM) and trans-impedance-mode (TIM)) from a broad viewpoint. So far, there are some research reports concerning OTA-based mixed-mode biquads [1-3]. But the OTA-based biquads above are not applicable to wideband behavior compared with the DVCC-based ones. If the mixed-mode biquad utilizing the PO-DVCCs is devised, the circuit has some excellent performances (i.e. wideband operation, low power dissipation, etc.) in comparison with conventional ones. However, such PO-DVCC-based biquad has not been well researched as yet.

This article focuses on a novel mixed-mode universal biquad using only the PO-DVCCs with grounded passive components as mentioned above. The biquad circuit configuration is consisted of an integrator loop structure with loss-less integrators [4]. The circuit performs the VM, CM, TAM and TIM operations with the selection of the input and output terminals, and it enables the low-pass (LP), band-pass (BP), high-pass (HP), band-stop (BS) and all-pass (AP) characteristics by suitably choosing the input signals with no component matching constraints. The characteristic parameters ω_0 and Q are set orthogonally by the circuit components. Additionally, the sensitivity analysis leads that the

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biquad has extremely low sensitivities with respect to circuit components.

A versatile mixed-mode biquad employing current controlled DVCCs (DVCCCs) is inducted. A DVCCC is an active device utilized effectively the parasitic resistance at the x-terminal of the DVCC. The circuit is composed of plus current output DVCCCs (PO-DVCCCs) and grounded capacitors. And the circuit performance can be controlled electronically with the bias currents of the PO-DVCCCs.

A biquad circuit design is carried out with PSPICE simulation, and the simulation responses are favorable sufficient over a wideband of frequencies. The biquad has several excellent performances in terms of the wideband operation, low power dissipation, orthogonal adjusting for the characteristic parameters, etc., and it suits well for CMOS implementation.

2. Plus current output DVCC

The symbol of the PO-DVCC is given in Figure 1, and hereinto it shows dual plus current output DVCC.

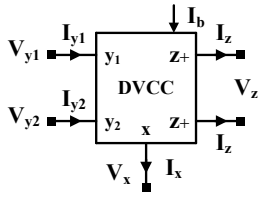

Figure 1: Symbolic representation of PO-DVCC

The PO-DVCC is characterized by the terminal equations [8] below:

$$V_x = V_{y1} - V_{y2}, \quad I_z = I_x \tag{1}$$

The MOS PO-DVCC configuration [11] is shown in Figure 2. It is an active device modified differential difference current conveyor (DDCC) [12], namely one y-terminal with plus polarity is grounded in the DDCC.

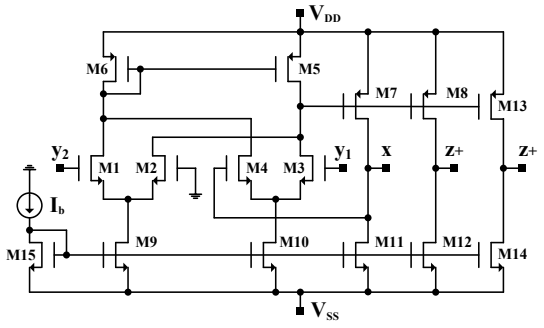

Figure 2: Plus current output DVCC configuration with MOS transistors

3. DVCC-based biquad and its performances

The mixed-mode universal biquad circuit configuration is shown in Figure 3. The circuit is consisted of four single PO-DVCCs, one dual PO-DVCC with grounded resistors and capacitors. This circuit is configured utilizing a second-order loss-less integrator loop structure [4].

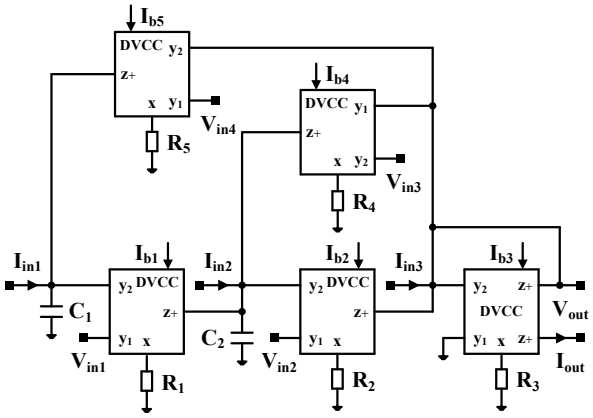

Figure 3: DVCC-based biquad circuit configuration

The voltage and current outputs $V_{out}(s)$, $I_{out}(s)$ are given as:

$$V_{out}(s) = \frac{N_v(s)}{D(s)} \tag{2} \qquad I_{out}(s) = \frac{N_i(s)}{D(s)} \tag{3}$$

where

$$N_v(s) = R_3[\{I_{in3}(s) + \frac{V_{in2}(s)}{R_2}\}s^2 - \frac{1}{C_2R_2}\{I_{in2}(s) + \frac{V_{in1}(s)}{R_1} - \frac{V_{in3}(s)}{R_4}\}s + \frac{1}{C_1C_2R_1R_2}\{I_{in1}(s) + \frac{V_{in4}(s)}{R_5}\}] \tag{4}$$

$$N_i(s) = -\frac{1}{R_3}N_v(s) \tag{5}$$

$$D(s) = s^2 + \frac{R_3}{C_2R_2R_4}s + \frac{R_3}{C_1C_2R_1R_2R_5} \tag{6}$$

It is obvious from the equations above that the circuit performs the mixed-mode behavior with the selection of the input and output terminals, and it enables the various kinds of the circuit responses choosing the input signals suitably.

In the CM operation (i.e. $V_{in1}(s)=V_{in2}(s)=V_{in3}(s)=V_{in4}(s)=0$), the circuit transfer functions are realized as below:

LP: $I_{in1}(s)=I_{in}(s)$, $I_{in2}(s)=I_{in3}(s)=0$

$$T_{LP}(s) = \frac{I_{out}(s)}{I_{in}(s)} = -\frac{1/C_1C_2R_1R_2}{D(s)} \tag{7}$$

BP: $I_{in2}(s)=I_{in}(s)$, $I_{in1}(s)=I_{in3}(s)=0$

$$T_{BP}(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{(1/C_2R_2)s}{D(s)} \tag{8}$$

HP: $I_{in3}(s)=I_{in}(s)$, $I_{in1}(s)=I_{in2}(s)=0$

$$T_{HP}(s) = \frac{I_{out}(s)}{I_{in}(s)} = -\frac{s^2}{D(s)} \tag{9}$$

BS: $I_{in1}(s)=I_{in3}(s)=I_{in}(s)$, $I_{in2}(s)=0$

$$T_{BS}(s)=\frac{I_{out}(s)}{I_{in}(s)}=-\frac{s^2+1/C_1C_2R_1R_2}{D(s)} \quad (10)$$

AP: $I_{in1}(s)=I_{in2}(s)=I_{in3}(s)=I_{in}(s)$

$$T_{AP}(s)=\frac{I_{out}(s)}{I_{in}(s)}=-\frac{s^2-(1/C_2R_2)s+1/C_1C_2R_1R_2}{D(s)} \quad (11)$$

The characteristic parameters ω_0 and Q are represented as:

$$\omega_0=\sqrt{\frac{R_3}{C_1C_2R_1R_2R_5}},\quad Q=R_4\sqrt{\frac{C_2R_2}{C_1R_1R_3R_5}} \quad (12)$$

Thus the circuit enables five basic circuit responses with no component matching constraints, and the characteristic parameters ω_0 and Q are set orthogonally by the passive components.

Especially the deviation of the circuit components affects the circuit performance. Hence we examine the effects with sensitivity analysis. The component sensitivities concerning ω_0 and Q are shown in Table 1. These values clarify that the circuit has low sensitive performance. It is an additional note that the sensitivities are not dependent on the component values.

Table 1: Component sensitivities

x	ω_0 sensitivity	Q sensitivity
R_1	-0.5	-0.5
R_2	-0.5	0.5
R_3	0.5	-0.5
R_4	0.0	1.0
R_5	-0.5	-0.5
C_1	-0.5	-0.5
C_2	-0.5	0.5

Successively we examine the performance of the VM circuit. The circuit responses in the VM operation (i.e. $I_{in1}(s)=I_{in2}(s)=I_{in3}(s)=0$) are found with the choice of the input voltages as below:

LP: $V_{in4}(s)=V_{in}(s)$, $V_{in1}(s)=V_{in2}(s)=V_{in3}(s)=0$

$$T_{LP}(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{R_3/C_1C_2R_1R_2R_5}{D(s)} \quad (13)$$

BP: $V_{in1}(s)=V_{in}(s)$, $V_{in2}(s)=V_{in3}(s)=V_{in4}(s)=0$

$$T_{BP}(s)=\frac{V_{out}(s)}{V_{in}(s)}=-\frac{(R_3/C_2R_1R_2)s}{D(s)} \quad (14)$$

HP: $V_{in2}(s)=V_{in}(s)$, $V_{in1}(s)=V_{in3}(s)=V_{in4}(s)=0$

$$T_{HP}(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{R_3}{R_2}\frac{s^2}{D(s)} \quad (15)$$

BS: $V_{in2}(s)=V_{in4}(s)=V_{in}(s)$, $V_{in1}(s)=V_{in3}(s)=0$

$$T_{BS}(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{R_3}{R_2}\frac{s^2+1/C_1C_2R_1R_5}{D(s)} \quad (16)$$

AP: $V_{in1}(s)=V_{in2}(s)=V_{in4}(s)=V_{in}(s)$, $V_{in3}(s)=0$

$$T_{AP}(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{R_3}{R_2}\frac{s^2-(1/C_2R_1)s+1/C_1C_2R_1R_5}{D(s)} \quad (17)$$

The VM circuit can also realize the LP, BP, HP, BS and AP transfer functions like as the CM one. The characteristic parameters ω_0, Q and component sensitivities are same as the current-mode ones.

In addition, the TAM and TIM operations are performed selecting the input terminal $I_{in}(s)/V_{in}(s)$ and output terminal $V_{out}(s)/I_{out}(s)$, respectively. Also, the circuit responses are derived with the above-mentioned ways in these operational modes.

4. Current controlled DVCC and biquad circuit configuration

In reality, the DVCC has parasitic resistance existing at the x-terminal, and the resistance varies with the bias current. The parasitic resistance R_x is given as:

$$R_x=K\left(\mu C_{ox}\frac{W}{L}I_b\right)^{-\frac{1}{2}} \quad (18)$$

where μ, C_{ox}, W/L, I_b and K denote the electron mobility, gate oxide capacitance per unit area, MOS transistor aspect ratio, bias current and constant parameter, respectively. Equation (18) shows that the parasitic resistance R_x is electronically adjusted with the bias current I_b. An active device made good use of the parasitic resistance is named DVCCC.

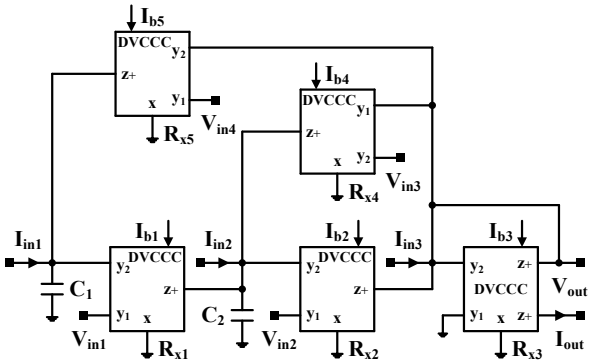

Figure 4: DVCCC-based biquad circuit configuration

Figure 4 illustrates the biquad circuit configuration employing the PO-DVCCCs. The circuit is composed of the PO-DVCCCs and grounded capacitors. The voltage and current outputs $V_{out}(s)$, $I_{out}(s)$ are given replacing the external resistance R_i to the parasitic resistance R_{xi} from (4) to (17). The characteristic parameters ω_0 and Q are also obtained with the same replacement.

The PO-DVCCC-based biquad has electronic tunability for the characteristic parameters with the bias currents. In addition, it can

be expected that the circuit has a high potential for low power performance, because the circuit configuration is without external resistors.

5. A circuit design and simulation responses

In order to confirm our proposal, we tried to realize a CM circuit using PSPICE simulation. As a circuit design, we deal a specification with the cut-off frequency f_0=1MHz, quality factor Q=1.0 and gain constant H=1.0. A macro model of the PO-DVCC in Figure 2 was used in this simulation.

To achieve the specification above, we set that the circuit components were R_i (i=1, 2, 3, 4, 5)=12kΩ and C_1=C_2=12pF, and that the bias currents (i=1, 2, 3, 4, 5)=10μA, DC supply voltages V_{DD}=-V_{SS}=0.8V and input current I_{in}=10μA, respectively.

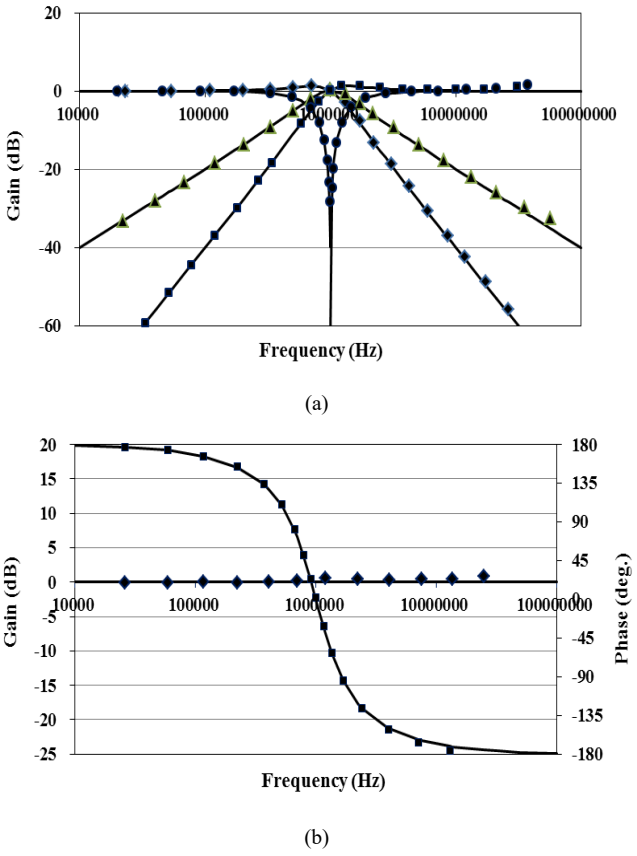

Figure 5: Simulated circuit responses

The simulation responses are given in Figure 5. Figure 5 (a) presents the LP, BP, HP and BS responses, and meanwhile the AP response is indicated in Figure 5 (b). In the figures, the marks signify the simulated responses, and the continuous lines show the theoretical responses. The simulated responses agree very well with the ideal values over a wide range of frequencies. The consumed power dissipation was 0.439mW. It's rather small.

The MOS transistor aspect ratios [10] are given in Table 2. Additionally, we utilized device parameters of MOSIS 0.5μm for other parameters.

Table 2: MOS transistor aspect ratios.

MOS transistors	W / L
M1-M4	20μm / 0.5μm
M5-M8, M13-M15	30μm / 2μm
M9-M12, M16-M19	10μm / 2μm

6. Conclusions

In this paper, we have proposed a novel mixed-mode universal biquad employing plus current output DVCCs with grounded passive components. Additionally, we demonstrated that the circuit accomplishes the mixed-mode behavior, and it enables five kinds of basic circuit responses without any component matching constraints. The circuit is capable of orthogonally adjusting the characteristic parameters by the circuit components. It has also been revealed that the component sensitivities were extremely low in the circuit.

The versatile plus current output DVCCC-based biquad has been inducted. The circuit can adjust electronically the circuit performances with the bias currents.

A circuit design was performed with SPICE simulation, and the simulated responses were sufficient good over a wideband of frequencies.

Our proposed biquad possesses several advantages concerning the wideband operation, low power dissipation, orthogonal adjusting for the characteristic parameters, etc., and it is easily capable of integrating in CMOS technology.

In reality, the DVCC has non-ideal elements (i.e. voltage and current tracking errors, etc.), and especially they affect the circuit performances. An appropriate solution on this must be found out in the future.

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