

# Multi-Objective Design of Current Conveyor using Optimization Algorithms

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## ABSTRACT

The design of microelectronic systems is often complex, therefore metaheuristics can be of a great interest, because in most cases these systems have conflicting objectives and constraints. In this paper, we demonstrate the application of multi-criteria design strategies to a CMOS current conveyor. This provides designers with the ability to develop solutions that can meet several objectives respecting the design constraints. Therefore, three evolutionary algorithms well-known for their best performance in the resolution of more difficult multi-objective problems are proposed. They are first applied to the well-known benchmark functions and then for the optimal design of the current conveyor transistors in the framework of the 0.18 $\mu$ m CMOS technology. The aim is to maximize the bandwidth and minimize the parasitic input resistance respecting the technological constraints of the circuit. The obtained results are integrated in Cadence tool to show their validities. Final performances obtained by the three methods are in agreement and are better compared to the state-of-art-results.

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## 1 Introduction

Today, with the complex growth of VLSI technology, it is very difficult to hand design analog integrated circuits with multiple parameters and purposes. The characterization of complicated trade-offs between conflicting and nonlinear performances while ensuring the required design specifications makes the design of analog circuits a tedious and time-consuming process. In this regard, due to their design difficulty and complexity, analog circuits have been attracted a lot of optimization attention. In general, optimization is often a time-consuming process having several contradictory criteria as well as a wide variety of design parameters. However, the design of electronic circuits is carried out by optimizing the circuit parameters to be able to rapidly design high-performance circuits [1]. For instance, finding passive elements values and transistor sizes and bias currents, so it can meet output performances such as gain, frequency band, power consumption, etc.

Several metaheuristics have been developed in the literature, which can be divided into two principal categories [2]: Single solution based methods, such as Taboo Search (TS) [3], Local Search (LS) [4], Simulated Annealing (SA) [5], or population based approaches like, Ant Colony Optimization (ACO)[6], Whale Op-

timization Algorithms (WOA)[7], Grey Wolf Optimizer (GWO), Particle Swarms Optimization (PSO)[8], Hybrid PSO-GWO [9], Non-dominated Sorting Genetic Algorithm (NSGA II)[10], Multi-objective Genetic Algorithm (MOGA)[11], Strength Pareto Evolutionary Algorithm (SPEA2)[12], etc. Single solution based techniques do not offer good results for problems where different types of variables, objectives and constraint functions (linear or non-linear constraints) are used [8]. Moreover, their efficiency highly depends on their parameters, the search space dimension and the number of variables. The population based techniques are generally classified into two groups, Particle Swarms (PS) and Evolutionary Algorithms (EA). PS give good results for problems that are not so difficult [13], but their performance also depends on their parameters and the complexity of the problem, especially for multi-objective optimization problems (MOP) [5, 13]. However, EAs are optimization techniques based on biological evolution and natural selection of species [14], are population-based, where each individual represents a possible solution. The initial population is generated randomly. At every new generation, the population iteratively evolves by the mutation, the crossover and the selection operators on each individual, and only non-dominated solutions meeting the constraints, will survive. Hence, such algorithms are well-known for their efficiency when

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solving complex MOP, Unlike PS, EAs do not need big parameter adjustments.

In this paper, we apply EAs for the optimal design of the current conveyor (CCII). The used EAs are NSGA II, MOGA and SPEA2, which allows the simultaneous optimization of multiple conflicting targets resulting into a set of Pareto Front (PF) solutions. Hence, the main objective to optimize the size of the MOS transistors transistors, using these algorithms, to achieve the high performances of the CCII. The CCII is one of the best known current mode circuits, making it the objective of several applications, such as filters, oscillators, etc., [15]. As far as we know, few works have been reported until now on CCII optimization by the EAs. In [16], the MOPSO with Crowding Distance (CD) was used for the optimization of the CCII, the differential CCII and the current feedback operational amplifier (CFOA) for low voltage low power applications, the MOPSO-CD was used as a part of a simulation-based tool to find the optimal sizing transistors that operate in weak inversion. In [17], the NSGA II and the decomposition-based multi-objective EA (MOEA/D) were used for the optimization of other purposes of the CCII, i.e., current gain and offset. However, the high-performance CCII design requires that the input parasitic resistance be small and its cut-off frequency be high. For this reason, we have chosen in this work these two characteristics as objectives to be optimized. All EAs generate Pareto fronts and simulations are carried out on Cadence using 0.18 $\mu\text{m}$  CMOS process. The simulation results are conform to those obtained by the optimization.

This paper is structured as follows: Section 2 gives an overview of the EAs, Section 3 is dedicated to the EAs validation using usual test functions. Section 4 presents the CMOS CCII. Section 5, is devoted to the results and discussion. A conclusion is given at the end.

## 2 Evolutionary Algorithms

### 2.1 MOGA

The MOGA was introduced in [11], as a new variant of the Golberg approach [18]. It uses the concept of dominance and a random-based fitness assignment. The non-dominated solutions are ranked into groups, which are assigned the same rank in each group.

The pseudo-code of MOGA is given by algorithm 1.

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#### Algorithm 1: MOGA Pseudo Code

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```

Generate the initial population  $P_i$ ;
Evaluate of  $P_i$ ;
while the stopping criteria is not met do
     $i=i+1$ ;
    Selection of  $P_i$ ;
    Mutation and Crossover of  $P_i$ ;
    Evaluate  $P_i$ ;
end
Result: non-dominated solutions

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### 2.2 NSGA II

NSGA-II, which was proposed in [10] as a modified version of NSGA, is among the most commonly used and effective EAs due to

its simplicity and effectiveness. The basic operation of the NSGA-II is : A random population is created. This generated population is sorted using the notion of dominance. A fitness function is assigned to each solution. Therefore, it is assumed that physical fitness is minimized. At first, selection, mutation and crossover operators are used to create a new population from the first. The NSGA II algorithm uses the notion of elitism, to compare the current population with previously found best non-dominated solutions.

NSGA II relies on two major procedures: crowding distance and fast non-dominated sorting. Both procedures ensure elitism and feasibility of solutions. Algorithm 2 represents the NSGA II pseudo-code.

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#### Algorithm 2: NSGA II Pseudo Code

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```

Generate randomly the initial population  $P_1$ 
while the stopping criteria is not satisfied do
    while population in not classified do
        Search for non-dominated individuals;
        Fitness calculation;
        Sharing;
    end
    Mutation;
    Crossover;
    Selection;
end

```

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### 2.3 SPEA2

SPEA2 is a MO algorithm introduced in [12] as an improved version of SPEA. It is based on the notion of dominating fitness evaluation to to generate the PF. SPEA2 uses elitist concept maintaining an external archive of non-dominated solutions. It also uses a nearest neighbor density estimation method, and an improved archive Truncation approach.

The SPEA2 is given by algorithm 3.

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#### Algorithm 3: SPEA2 Pseudo Code

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```

Generate randomly population  $P_i$ ;
Evaluate objective and create external Archive  $A_i$  ;
for  $i = 1, i \leq \text{Max iterations}$  do
     $i=i+1$ ;
    Evaluate objectives and update  $A_i$  by Truncation
    operator;
    Perform Binary Tournament Selection ;
    Crossover of  $P_i$  ;
    mutation of  $P_i$  ;
end
Result: External Archive with non dominated solutions.

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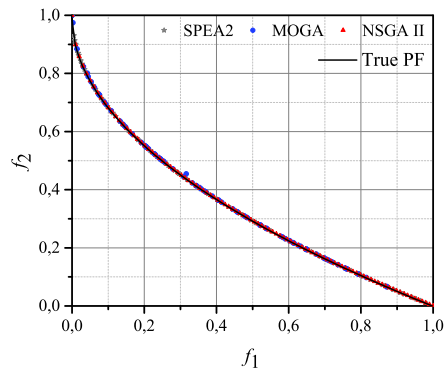
## 3 EA robustness

Before using the proposed algorithms, we evaluated performances using multi-objective standards ZDT functions [19].

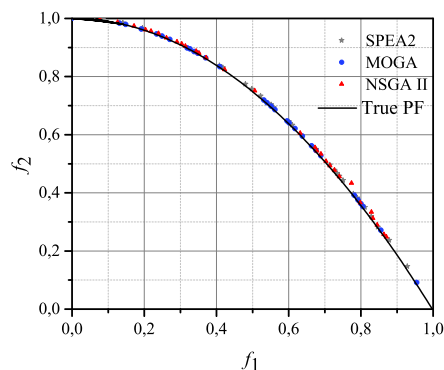
Each ZDT function includes two objectives  $f_1$  and  $f_2$  with 30 variables, which demonstrates the high complexity of such test functions. All tests are carried out with the algorithms parameters of

1000 iterations and a population size of 50 and a crossover probability of 0.8 and a mutation probability of 0.1. The ZDT benchmark functions and their expressions are given in the appendix.

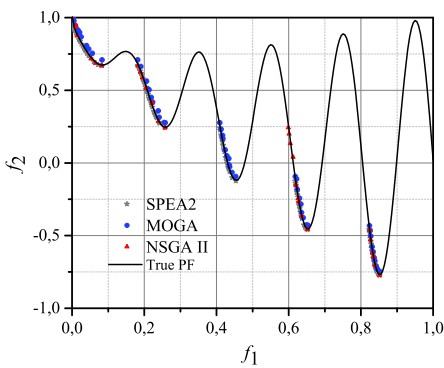
Figure 1 shows the PFs obtained for the three chosen algorithms. As can be clearly seen the generated PFs with the all proposed methods achieve good approximations to the exact benchmark functions PFs. Therefore, we can confidently use them for the optimization problems of the CCII optimal design with guaranteed results.



(a) ZDT1



(b) ZDT2



(c) ZDT3

Figure 1: Evaluation of algorithms by ZDT benchmark functions

## 4 CMOS Current Conveyor

In this section, we studied the current conveyor shown in Figure 2, it has three active ports X, Y and Z, and its main function consists of

- Current follower between ports X and Z, which can be provided by the translinear loop formed by transistors M1- M4.
- Voltage follower between ports X and Y, which can be provided by M5-M6 and M7-M8 current mirrors.

The present current conveyor topology is the most used one for its good performances and the interest of using a translinear loop [20]. Therefore, the design optimization of the CCII is performed considering its main objective functions : the parasitic resistance at the port X ( $R_X$ ) and the cut-off frequency ( $f_{-3dB}$ ). Recall that the aim is to minimize the first objective to obtain low input resistance and to maximize the second objective to get high bandwidth.

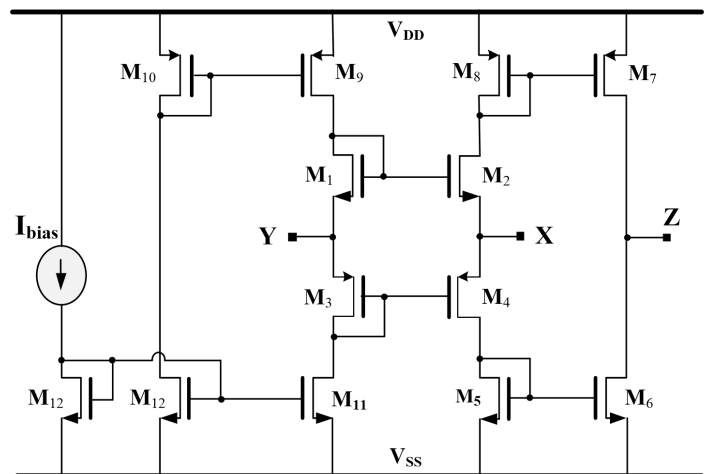


Figure 2: CMOS Current conveyor.

The CCII sizing is performed as in [14], using CMOS 0.18  $\mu\text{m}$  process, and with the following conditions  $V_{DD} = V_{SS} = \pm 1.8\text{V}$ . All the transistors are characterized by their geometrical parameters: the channel length  $L$  and the gate width  $W$ .

The CCII optimal sizing issue is treated as a MOP. The aim is to find the best trade-off between a small  $R_X$  and a high  $f_{-3dB}$  as a function of the transistors parameters. The problem constraints are given by Eqs. 4 and 5 bellow corresponding to the saturation transistor regime [15].

The design problem can be formulated as:

$$\begin{aligned} \text{Minimize } & R_X(x) \text{ and } -f_{-3dB}(x). \\ & x = \{W_n, W_p, L_n, L_p, I_0\}. \end{aligned}$$

(1)

subject to

$$g_{1,2}(x) \leq 0,$$

where

- The resistance  $R_X$  is

$$R_X = \frac{1}{g_{mn} + g_{mp}} = \frac{1}{\sqrt{2\mu_n C_{ox} \frac{W_n}{L_n} I_0} + \sqrt{2\mu_p C_{ox} \frac{W_p}{L_p} I_0}} \quad (2)$$

$g_{mn(p)}$  is the transconductance for N(P) channel transistor.  $\mu_n$  ( $\mu_p$ ) and  $C_{ox}$  are the electrons (holes) mobility and the gate oxide capacitance per unit area, respectively.  $I_0$  is the bias current.

- The cut-off frequency  $f_{-3dB}$  is

$$f_{-3dB} = \frac{\omega_{-3dB}}{2\pi} \quad (3)$$

The saturation constraints  $g_1$  and  $g_2$  are given by :

- The constraint of  $M_2$  and  $M_8$  transistors:

$$g_1 = V_{SS} - V_x(\min) + V_{tn} + \sqrt{\frac{2I_0}{\mu_n C_{ox} \frac{W_n}{L_n}}} + \sqrt{\frac{2I_0}{\mu_p C_{ox} \frac{W_p}{L_p}}} \quad (4)$$

- The constraint of  $M_4$  and  $M_5$  transistors:

$$g_2 = V_x(\max) - V_{DD} - V_{tp} + \sqrt{\frac{2I_0}{\mu_n C_{ox} \frac{W_n}{L_n}}} + \sqrt{\frac{2I_0}{\mu_p C_{ox} \frac{W_p}{L_p}}} \quad (5)$$

where  $V_{tn}(V_{tp})$ ,  $V_{DD}(V_{SS})$  are the threshold voltage for NMOS(PMOS) and the supply voltage, respectively.  $W_n$  ( $W_p$ ),  $L_n$  ( $L_p$ ) are the gate width and the channel length for n-channel (p-channel) transistors, respectively.

## 5 Results and discussion

All the CCII transistors with the same channel type have the same parameters ( $W_n$ ,  $L_n$  for NMOS and  $W_p$ ,  $L_p$  for PMOS). To respect the industrial design constraints, we also used identical channel length ( $L$ ) for all transistors.

### 5.1 CCII optimization results

The optimal MOS transistors sizes are reached using EAs by minimizing  $R_X$  and maximizing  $f_{-3dB}$  in two ways:

First, the optimization process is performed by MOGA, SPEA2 and NSGA II using three  $I_0$  values, i.e.,  $20\mu A$ ,  $40\mu A$  and  $80\mu A$ . For these experiments, we use the minimum channel length  $L_n = L_p = L_{min}$ . The generated PFs ( $R_X$  and  $-f_{-3dB}$ ) by the algorithms for different bias currents are shown in Figure 3. From this figure, we can see that the best trade-off between  $R_X$  and  $-f_{-3dB}$  is obtained for the PF with the large bias current  $I_0=80\mu A$ . Therefore, designers have to select the best trade-off solution depending on the circuit design and its application requirements.

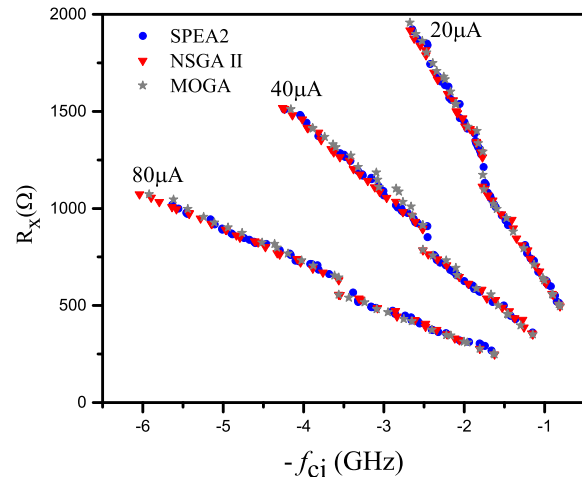


Figure 3: Pareto fronts obtained by the three algorithms for three bias currents

Second, the optimization process is performed by the same algorithms using three channel lengths  $L_{min}$ ,  $2L_{min}$  and  $3L_{min}$ . For these experiments, we use  $I_0 = 80\mu A$ . The generated PFs for these cases are shown in Figure 4. From this figure, we can see that the best trade-off between performances is achieved for the PF with a minimum channel length  $L_{min}$ . Unlike digital circuits, the channel length for analog circuits is usually at least  $3L_{min}$ , which is why we tested all three channel lengths. This relatively large channel lengths minimizes the effects of channel modulation.

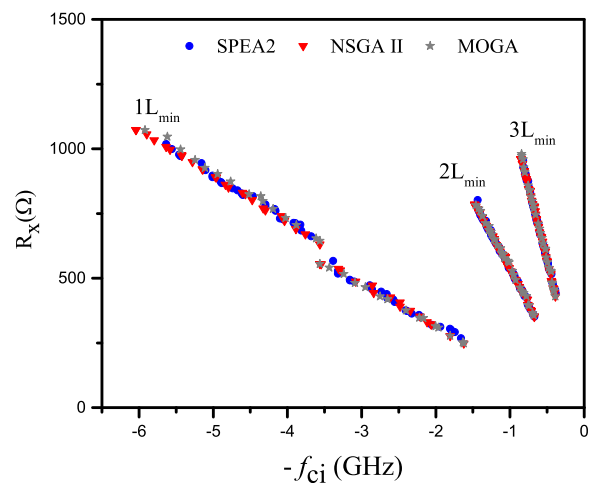


Figure 4: Pareto fronts obtained by the three algorithms for three channel lengths.

Based on the results in both scenarios, we can see that the best performances are obtained with a smaller channel length and a higher bias current. Considering the effects of channel modulation, power consumption and the circuit design and application requirements, IC designers should select the appropriate solution.

We run all algorithms 10 times, to evaluate the weakness and strength of each algorithm in all the performed experiments. To evaluate the diversity and the distribution of Pareto solutions, we

use the hyper volume metric [21]. This metric shows the covered area by the Pareto front. In case of minimization, of the problem, the larger hyper-volume value, the good is the quality of Pareto front solutions.

The hypervolume results are shown in Table 1. The optimization procedure required a mean CPU time of approximately 6.707 s, 67.25 s, and 148.412 s for NSGA II, MOGA and SPEA2, respectively.

Compared to the others algorithms, the NSGA II has the rapid CPU time and a good convergence rate confirmed by the higher hypervolume value.

Table 1: The Hypervolume Values.

		SPEA2	MOGA	NSGA II
$L_{min}$	20 $\mu\text{A}$	0.750	<b>0.752</b>	<b>0.752</b>
	40 $\mu\text{A}$	0.825	0.824	<b>0.826</b>
	80 $\mu\text{A}$	0.873	0.875	<b>0.876</b>
80 $\mu\text{A}$	1 $L_{min}$	0.873	0.875	<b>0.876</b>
	2 $L_{min}$	0.824	0.823	<b>0.825</b>
	3 $L_{min}$	0.782	0.784	<b>0.785</b>

### 5.2 CCII validation results

Table 2 presents the solutions to be validated by the CADENCE tool, they are defined by their cutoff frequencies, their values of  $R_X$  and the corresponding transistors parameters. They are randomly chosen from the PF that corresponds to  $I_0 = 80\mu\text{A}$  and  $L_n=L_p=L_{min}$ .

Table 2: Parameters to be validated by Cadence, obtained in the PF that gives the best trade-off ( $R_X, f_{3dB}$ ).

	Test	$W_n(\mu\text{m})$	$W_p(\mu\text{m})$	$f_{3dB}(\text{GHz})$	$R_X(\Omega)$
MOGA	1	1.08	4.26	5.11	926.5
	2	3.77	13.38	3.08	481.26
SPEA2	1	0.86	3.54	5.63	1018.6
	2	4.30	17.85	2.66	439.07
NSGA II	1	0.80	3.08	6.04	1073.3
	2	4.65	15.77	2.64	443.26

Figures 5–8 show the simulation results of the selected solutions in table 2. The maximum (minimum) deviation between the simulation and the theoretical results is 10.1% (1%) and 9.4% (4.7%) for  $R_X$  and  $f_{3dB}$ , respectively. This interval of variations is quite narrow and makes it possible to consider that the simulation results are in good agreement with the theoretical ones, obtained by the algorithms.

Table 3 presents a qualitative comparison of the obtained CCII performance with works previously published but with 0.35 $\mu\text{m}$  process. From the data given in this table, it is clear that the achieved performances are higher than reported, i.e, very higher frequency and much lower power consumption and good X-port resistance.

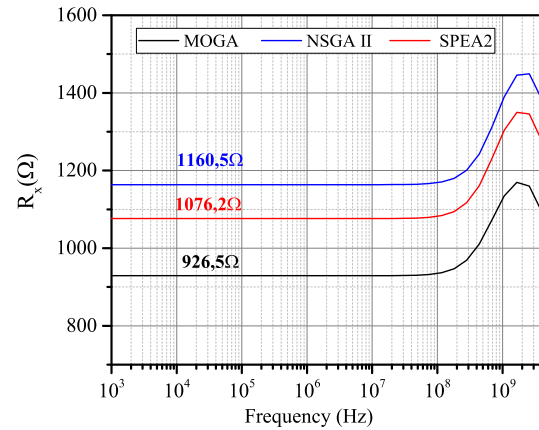


Figure 5: Cadence simulation results of parasitic resistance for the used algorithms (Tests 1 in table 2).

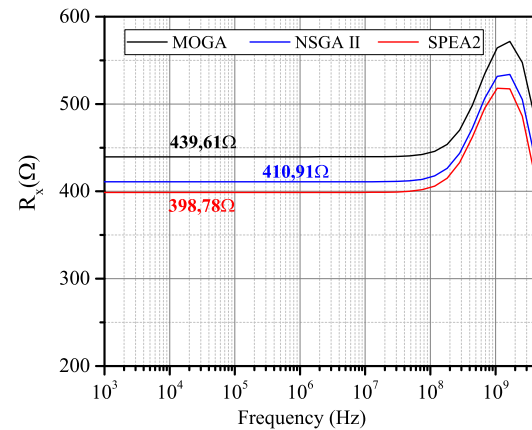


Figure 6: Cadence simulation results of parasitic resistance for the used algorithms (Tests 2 in table 2).

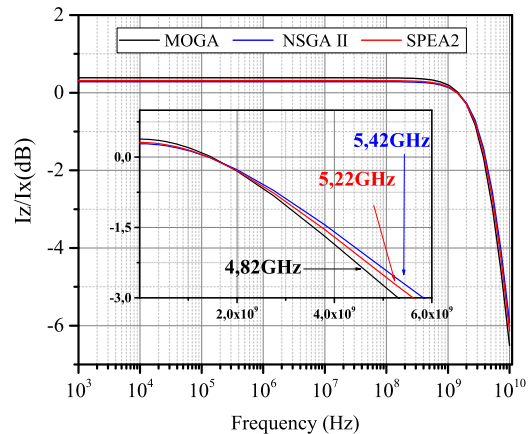


Figure 7: Cadence simulation results of cut-off frequency for the used algorithms (Tests 1 in table 2).

Table 3: CCII performance comparison with works previously published.

	This work	[22]	[23]	[24]
Algorithms	NSGA II	PSO-2S	MODE	EGO-PEI
Technology (μm)	CMOS 0.18	CMOS 0.35	CMOS 0.35	AMS 0.35
V <sub>DD</sub> /V <sub>SS</sub> (V)	±1.8	±2.5	±2.5	–
I <sub>bias</sub> (μA )	80	300	300	–
Power (μW )	288	1500	1500	–
f <sub>-3dB</sub> (max) (GHz)	6.04	2.121	2.132	1.2255
R <sub>x</sub> (min) ( Ω )	247	225	221	259.53

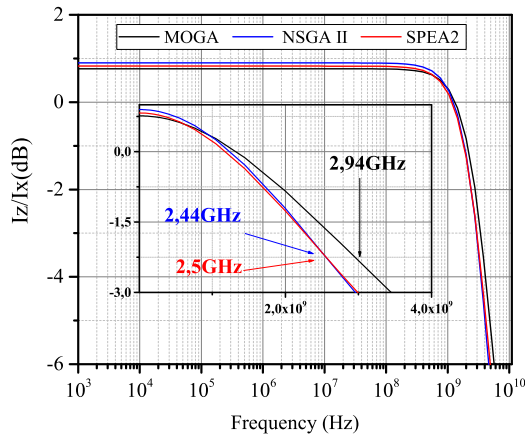


Figure 8: Cadence simulation results of cut-off frequency for the used algorithms (Tests 2 in table 2).

## 6 Conclusion

In this paper, we presented the usefulness of applying EAs, namely MOGA, SPEA2 and NSGA II, for the automatic optimization of high performances CCII. Several optimization experiments were carried out with three bias currents and three channel lengths, minimizing the parasitic resistance and maximizing the cut-off frequency. In all experiments, the achieved results show that these methods can provide Pareto Fronts with greater solutions diversity. The simulations are performed by Cadence using the CMOS 0.18μm process, showing good accuracy with the theoretical results. The best performances achieved with EAs in this work can be summarized in a power consumption of 288μW, a minimum parasitic resistance of about 247Ω and a maximum frequency of about 6.04GHz.

### Appendix

- ZDT1 function:

$$g(\vec{x}) = 1 + 9 \sum_{i=2}^{Dim} \frac{x_i}{30-1} \quad \text{and} \quad h(\vec{x}, f_1, g) = 1 - \sqrt{\frac{f_1(\vec{x})}{g(\vec{x})}} \quad (6)$$

$$f_1(\vec{x}) = x_1$$

$$f_2(\vec{x}) = g(\vec{x}).h(\vec{x}, f_1, g)$$

- ZDT2 function:

$$g(\vec{x}) = 1 + 9 \sum_{i=2}^{Dim} \frac{x_i}{30-1} \quad \text{and} \quad h(\vec{x}, f_1, g) = 1 - \left( \frac{f_1(\vec{x})}{g(\vec{x})} \right)^2 \quad (7)$$

$$f_1(\vec{x}) = x_1$$

$$f_2(\vec{x}) = g(\vec{x}).h(\vec{x}, f_1, g)$$

- ZDT3 function:

$$g(\vec{x}) = 1 + 9 \sum_{i=2}^{Dim} \frac{x_i}{30-1}$$

$$h(\vec{x}, f_1, g) = 1 - \left( \frac{f_1(\vec{x})}{g(\vec{x})} \right) \sin(10\pi f_1(\vec{x})) - \sqrt{\frac{f_1(\vec{x})}{g(\vec{x})}} \quad (8)$$

$$f_1(\vec{x}) = x_1$$

$$f_2(\vec{x}) = g(\vec{x}).h(\vec{x}, f_1, g)$$

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