ASTES

Advances in Science, Technology and Engineering Systems Journal
Vol. 5, No. 1, 285-293 (2020)
www.astesj.com
Special Issue on Multidisciplinary Sciences and Engineering

ASTES Journal
ISSN: 2415-6698

Implementation of Paraconsistent Logic Based PI Controller for TA Converter

Tapas Kumar Mohapatra*, Asim Kumar Dey, Krushna Keshab Mohapatra

SOA University, Department of Electrical Engineering, 751030, India

ARTICLE INFO

Article history:
Received: 14 October, 2019
Accepted: 23 January, 2020
Online: 10 February, 2020

Keywords:
Photo Voltaic (PV)
Paraconsistent Logic (PL)
Positive output voltage
TA converter
Paraconsistent logic based PI (PLPI)

ABSTRACT

A novel control technique is implemented for TA converter. This converter is used for charging of electric vehicle Battery from a Photo Voltaic (PV) Module. TA converter is one type of non-isolated buck-boost converter. This converter provides positive output voltage. This article is an extension work that is originally presented in 2019 IEEE International Conference on Sustainable Energy Technologies (ICSET). A Comparative study of the performances of different converters has been described. The Paraconsistent Logic (PL) is used for a PI controller. The performance of new Paraconsistent Logic based PI (PLPI) controller is compared with the conventional PI controller. This control has the similar action as PI and the logical actions as structured in Paraconsistent Logic. Operational details of TA converter with the different performances has been described in this article. MATLAB is used to validate the performance by developing both state space and simulation model. The robustness of the controller is compared with traditional PI controller. The hardware of the TA converter with the new PLPI control technique is projected and also matched with simulation results.

1 Introduction

Because of extraordinary utilization of petroleum derivative and air contamination, the auto mobile sectors are compelled to consider electric vehicles (EV). Presently a days EV battery modelling and its charging is an extraordinary research region. It is notable, switch mode power supply (SMPS) is the core of power transformation innovation. EV battery charging is promising through simple and efficient DC-DC converter. Mostly buck-boost converter is preferred for the EV battery charging process. Buck and boost converters are simple and efficient but unable to provide high voltage gain. Multiple circuits have been projected in different articles such as the complex topology developed by LUO [1]–[3] provides a high voltage gain. It is costly, big in size and losses is also more. Interleaved converters [4]–[10] are able to provide high voltage gain with less voltage stress but their operational mode ,converter arrangement and control strategies are very complex. Hwu and Peng [10] also developed buck-boost topology which can provide voltage gain of 2D with positive output. Quadratic converters [11] – [14] can provide high voltage gain with less efficiency. KY converter [15] has high voltage gain but increases complexity with additional switches and also increases the overall cost.Though the traditional buck-boost converter introduce high efficiency with reduced cost but unable to provide higher and positive output voltage. In 1991 Cuk suggested a converter, [16] which is able to provide a voltage gain of $\frac{D^2}{(1-D)^2}$ but can only operate in buck mode due to the presence of clamping diode D_1 and D_2. The converter which provides low gain can provide high or low voltage output at very high or very low duty ratio, which is practically difficult to achieve. A new converter proposed in [17], having little voltage ripple, negligible radio frequency intervention, and one shared ground switch but complexity increases due to the 7^{th} circuit and also having different ground in its input and output terminals. In [18], a cascaded converter, combining two separated converters with both current source and sink, is functional for the thermoelectric generator. However, the voltage gain is also unnatural. Particularly, in order to attain high-voltage gain, the above converters must be functioning under extremely high or little duty cycle which is difficult to realize due to the practical limitations. Therefore, discovering new converter topology to overcome the negatives of the conventional ones for the requirements in industries is significant and appreciated.

TA converter [19] is proposed in the article which is one type non isolated positive output based buck-boost converter. It introduce a voltage gain of $\frac{D^2}{(1-D)^2}$. Though the voltage gain is similar to several other proposed converters but it disables few problems associated with others. This TA converter has several advantages over Shan and Faqiang converter [20] like:

*Tapas Kumar Mohapatra , Dept. of Electrical Engineering, SOA University & tapasmohapatra@soa.ac.in

- High voltage gain with positive output voltage.
- Less current stress in capacitor.
- Less voltage stress in inductor.
- Less source current for same load current in comparison to others.
- Can operate at CCM mode at low switching frequency.

The basic range of battery used for electric bike varies between 12 to 48 volt. In this article a battery of 12 volt, 7AH rating is used as a load, which is charged from a source varies between 6 to 30 volt. TA converter with PI controller is used to provide a constant voltage of 12 volt from a solar panel.

A controller/regulator is basically act as the brain of the system. Three types of conventional controller such as Proportional, Proportional and Integral (PI) and Proportional, Integral and Derivative (PID) have a wide scope of uses in SMPS application. With scientific advancement, controllers got computational assets about the 1980s, and turned out to be increasingly productive. The incorporation of micro controller chips for the implementation of controllers, in DC to DC converters, allowing the integration of algorithms with P, PI and PID activities, the expansion of structures with automatic tuning and massive simplicity in control parameter settings [21] - [24]. The primary goal of this work is to introduce the consequences of the PI controller using PL in the novel DC to DC boost converter and also compare the result with the conventional PI controller.

In section II of the article, the converter circuit diagram, operation and analysis is explained. Mathematical model and Simulink model is revealed in section III. In section IV, the Paraconsistent Logic based PI controller (PLPI) is explained. In section V hardware and simulation result of the converter is compared for PL-PI as well as the results compared with other converters. In the section VI the dynamic performance of the proposed controller is compared with conventional PI controller. Few comments and concluding remarks are given in section VII

2 Proposed TA converter Structure, Operation and analysis

2.1 Structure / Circuit Diagram

TA converter circuit diagram is shown in figure-1. The circuit elements of the converter are as follows: S_1 and S_2) - Power switches,(D_1 and D_2) – Diodes, (L_1 and L_1)- Inductors, (C_1 and C_1) - Capacitors. Time domain wave forms of the TA converter in CCM is shown in figure-3.

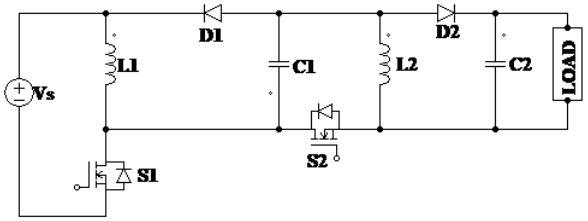


Figure 1: Circuit diagram of TA converter

2.2 Operating Principle and Analysis

In continuous conduction mode (CCM) the converter drives in two modes. First Mode -(0 < t < DT): In first mode S_1 and S_2 switches are simultaneously turned on and acts as short circuit, D_1 and D_2 diodes get reverse biased and act as open circuit. The direction of inductor currents are shown in figure - 2(a). C_2 provides the necessary output power to load. The following dynamic equations (1 - 8 will be obtained from figure - 2(a).

$$V_s - L_1\frac{di_{L1}}{dt} = 0 \quad (1)$$

$$\int_{I_{L1min}}^{I_{L1max}} di_{L1} = \int_0^{DT} \frac{V_s}{L_1} \quad (2)$$

$$\Delta I_{L1} = \frac{V_S}{L_1}DT \quad (3)$$

$$V_s - V_{L1} = 0 \quad (4)$$

$$V_{C1} - L_2\frac{di_{L2}}{dt} = 0 \quad (5)$$

$$\int_{I_{L2\min}}^{I_{L2\max}} di_{L2} = \int_0^{DT} \frac{V_{C1}}{L_2}dt \quad (6)$$

$$\Delta I_{L2} = \frac{V_{C1}}{L_2}DT \quad (7)$$

$$V_{C1} - V_{L1} = 0 \quad (8)$$

Second Mode - (0 < t < (1-D)T): In second mode S_1 and S_2 switches are simultaneously turned off and acts as open circuit, D_1 and D_2 diodes get forward biased by the inductors and act as short circuit. The direction of inductor currents are shown in Figure - 2(b). Inductor provides the necessary output power to load and to charge the capacitor C_2. The following dynamic equations (9 - 16) will be obtained from figure-2(b).

$$-V_{C1} - L_1\frac{di_{L1}}{dt} = 0 \quad (9)$$

$$\int_{I_{L1\max}}^{I_{L1\min}} di_{L1} = \int_0^{(1-D)T} \frac{-V_{C1}}{L_1}dt \quad (10)$$

$$\Delta I_{L1} = \frac{V_{C1}}{L_1}(1-D)T \quad (11)$$

$$-V_{C1} - V_{L1} = 0 \quad (12)$$

$$-V_{C2} - L_2\frac{di_{L2}}{dt} = 0 \quad (13)$$

$$\int_{I_{L2\max}}^{I_{L2\min}} di_{L2} = \int_0^{(1-D)T} \frac{-V_{C2}}{L_2}dt \quad (14)$$

$$\Delta I_{L2} = \frac{V_{C2}}{L_2}(1-D)T \quad (15)$$

$$-V_{C2} - V_{L2} = 0 \quad (16)$$

As we know the inductor voltage over a period is zero. We will obtain the following relations as given in equations (17-19). The inductor currents and capacitor voltages ripple are written in equation (20-23). Where f_{SW} is the switching frequency.

$$V_{C2} = V_0 = V_{C1}\frac{D}{1-D} \quad (17)$$

$$V_{C1} = V_S\frac{D}{1-D} \quad (18)$$

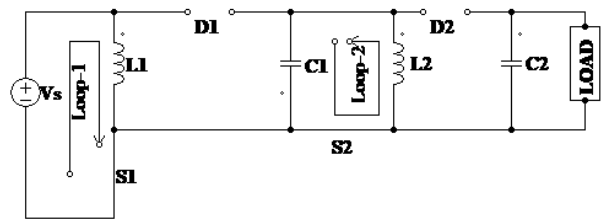
$$V_0 = V_S\frac{D^2}{(1-D)^2} \quad (19)$$

$$\Delta I_{L1} = \frac{V_S D}{L_1 f_{Sw}} \quad (20)$$

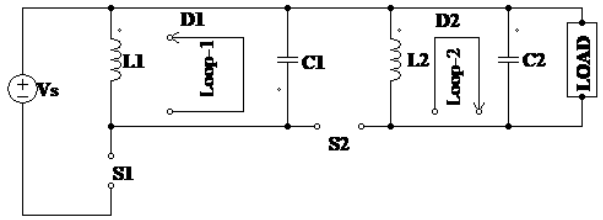
$$\Delta I_{L2} = \frac{V_S D^2}{L_2 f_{Sw}(1-D)} \quad (21)$$

$$\Delta V_{C1} = \frac{V_0 D}{RC_1 f_{Sw}(1-D)} \quad (22)$$

$$\Delta V_C 2 = \frac{V_0 D}{RC_2 f_{Sw}} \quad (23)$$



(a) First Mode



(b) Second Mode

Figure 2: Equivalent circuit diagram of two modes of TA converter

3 TA converter mathematical and simulink model

3.1 State Space Model

From the Mode-I and Mode-II the following dynamic equation will be obtained using which the state model can be obtained. The equations are given in (24-31).

$$\frac{di_{L1}}{dt} = \frac{V_S}{L_1} \quad (24) \qquad \frac{di_{L1}}{dt} = \frac{-V_{C1}}{L_1} \quad (28)$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1}}{L_2} \quad (25) \qquad \frac{di_{L2}}{dt} = -\frac{V_{C2}}{L_2} \quad (29)$$

$$\frac{dV_{C2}}{dt} = -\frac{V_{C2}}{RC_2} \quad (26) \qquad \frac{dV_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{V_{C2}}{RC_2} \quad (30)$$

$$\frac{dV_{C1}}{dt} = i_{L2} \quad (27) \qquad \frac{dV_{C1}}{dt} = -i_{L1} \quad (31)$$

$$\frac{di_{L1}}{dt} = D\frac{V_S}{L_1} - (1-D)\frac{V_{C1}}{L_1} \quad (32)$$

$$\frac{di_{L2}}{dt} = D\frac{V_{C1}}{L_2} - (1-D)\frac{V_{C2}}{L_2} \quad (33)$$

$$\frac{dV_{C2}}{dt} = -D\frac{V_{C2}}{RC_2} + (1-D)\frac{i_{L2}}{C_2} - (1-D)\frac{V_{C2}}{RC_2} \quad (34)$$

$$\frac{dV_{C1}}{dt} = Di_{L2} - (1-D)i_{L1} \quad (35)$$

The average model is given in equations (32-35).From the above equation it is clearly visible that the system is a fourth order one.

3.2 Simulation model and results

Figure-4 shows the Simulink model of the projected buck boost converter with PLPI controller. The circuit parameters that are used in the Simulink model are given in Table-II. Only one gate signal is essential for both the switches as both of them are operating simultaneously. A source of 18 volt is applied with output voltage of 40 volt in boost mode and 14 volt in buck mode. Input voltage is varied from 4volt to 18volt in boost mode and 18 volt to 100 volt in buck mode for the verification of robustness. Load resistance is also varied from 40Ω to 160Ω in boost and 5Ω to 50Ω in buck mode for the same verification. The load voltage remains as required with the above voltage and load resistance variations. In the figure -5 currents of each inductor and source, voltages of each capacitor, switch and diodes in boost mode are shown. Similarly in figure -6 the above waveforms in buck mode are displayed. It is clearly visible from figure - 5 and figure - 6 that i_{L1} never goes to negative value for both mode of operation.

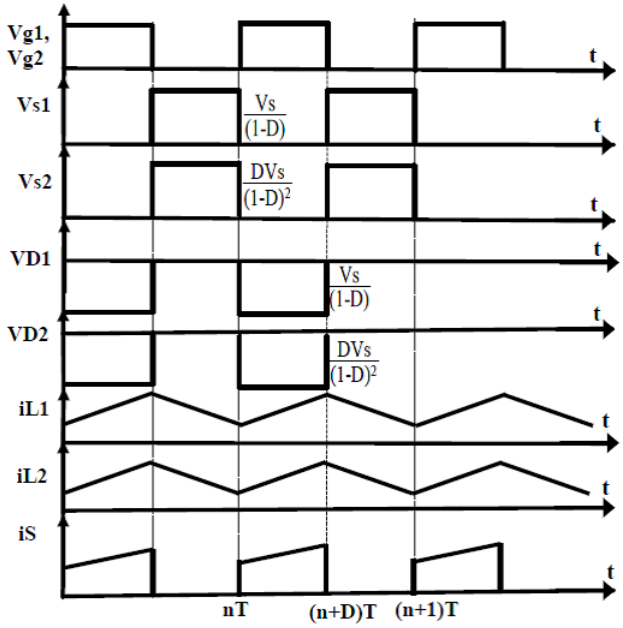


Figure 3: Different voltage and current wave forms

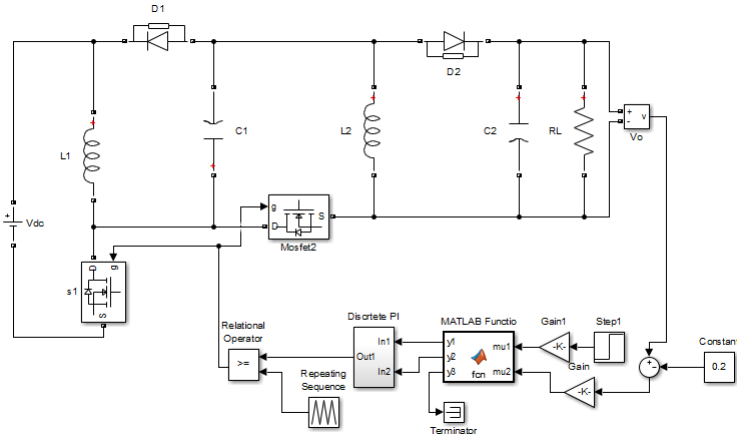


Figure 4: Matlab simulink model of proposed TA converter

4 Paraconsistent logic based PI controller

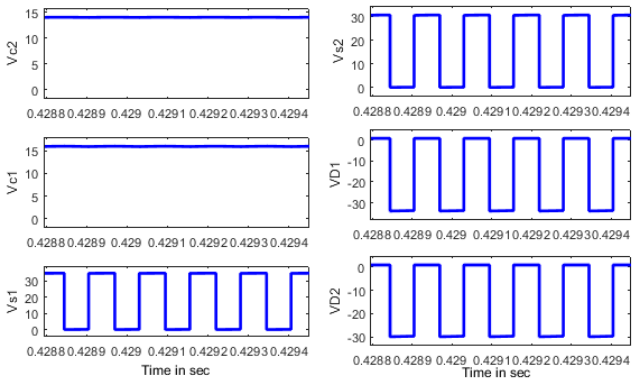
4.1 Logic of paraconsistent.

The conventional or Aristotelian logic underpins our present innovation is created on rigid binary laws and, along these lines, does not concede circumstances of redundancy, irregularities or those that are communicated by deficiency [25]. In conventional logic there is no logical inconsistency like something can't be both genuine and not valid in the meantime, when dealing with similar context. In any

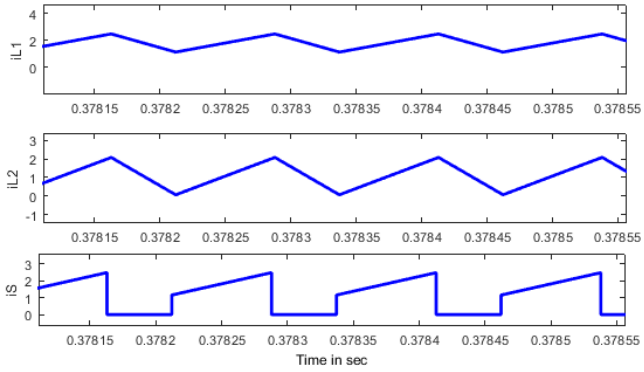
case, with the cut-off points of measures of control and eminence at present mandatory, progressively polished, make the philosophies of Conventional logic difficult to give effective control prototypes so improved for this mandate [25]. So as to act in circumstances where binary logic is difficult to be connected, different sorts of logic, called non-conventional, for example, Fuzzy, multivalued, paraconsistent, and so on, have as of late been made [25] - [26].

Non-conventional logics have the primary target is to restrict the binary principle of conventional logic and also catch diverse parts of casual conflicts. For instance, the principle of non-contradiction (PNC) in conventional logic explains that conflicting articulations can't both be valid in a similar sense in the meantime. Be that as it may, on account of signals as for a physical quantity beginning from two sensors, they might be conflicting, which gives conflicting data to make decision. In this way, control system will be progressively effective on the off chance that they are ready to act in circumstances where data might be conflicting.

A non-conventional Paraconsistent (PL) logic property states that it can tolerate the logical inconsistency in its establishments and is capable of managing conflicting signals. The PL has as its expansion the Paraconsistent Annotated Logic (PAL), which has a Hasse (Lattice FOUR) related with logical states existing at its vertices. Along these lines, sentences can be acquired where recommendations can be examined based on confirmations. In this PAL portrayal, the four extraordinary logic existing at the vertices of the PAL lattice are: Paracomplete ($\perp$), False (f), True (t) and Inconsistent ($\top$) [27] - [28].

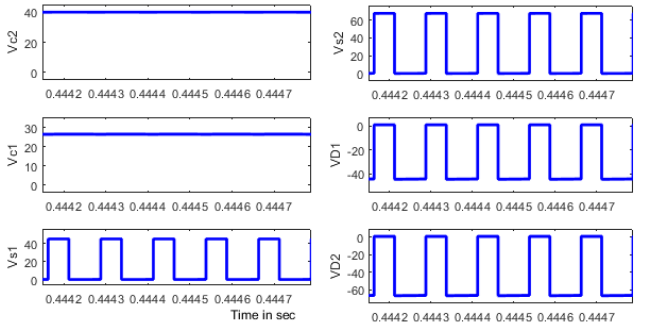


(a) $V_{c2}, V_{c1}, Vs1, V_{s2}, V_{D1}$ and V_{D2}

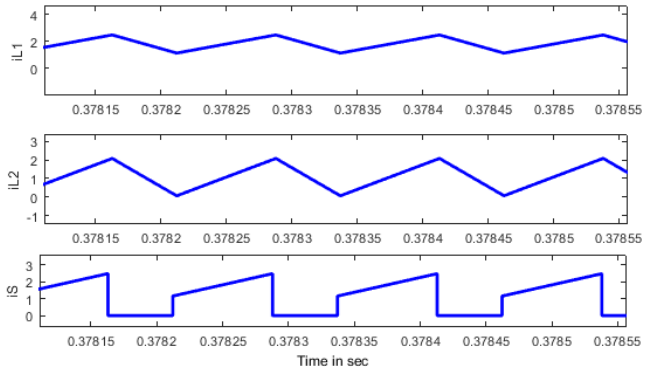


(b) $i_{L1}, i_{L2} and i_S$

Figure 6: Simulation result of TA converter in buck mode

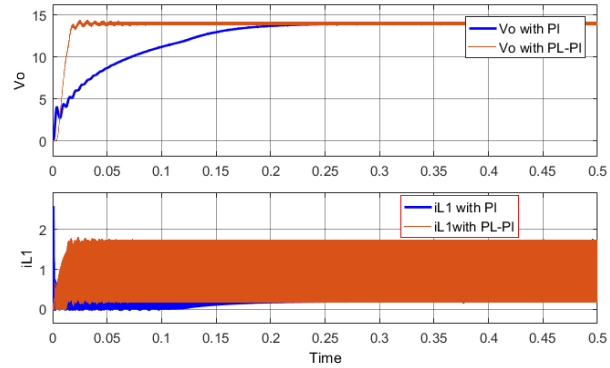


(a) $V_{c2}, V_{c1}, Vs1, V_{s2}, V_{D1}$ and V_{D2}

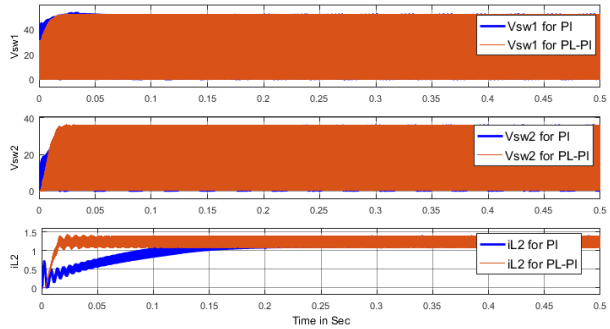


(b) $i_{L1}, i_{L2} and i_S$

Figure 5: Simulation result of TA converter in boost mode



(a) V_0 and i_{L1}



(b) $V_{sw1}, V_{sw2} and i_{L2}$

Figure 7: Comparison of results with PI and PL-PI

4.2 Logic with annotation of two values.

From a Lattice of four vertices it is conceivable to relate a sort of Paraconsistent Annotated Logic in which two evidential qualities related to a specific suggestion are considered. By translating the evidential values by methods for comment or standardized degrees of proof we can acquire conditions including the logical states that are characterized with degrees of proof from estimations. This sort of logic is called Paraconsistent Annotated Logic with explanation of two values (PAL2v) [27] - [28]. Figure-8(a) demonstrates the Lattice FOUR related at PAL2v.

In PAL2v an evidential nuclear equation of the shape P (μ , λ) can be viewed as an explanation for the recommendation p, where μ , $\lambda \in [0, 1]$ (genuine unit interim) [26] - [27]. Along these lines, the Evidence degree (μ) is an esteem that speaks to the proof ideal to the recommendation p, and the Evidence degree (λ) is an esteem that speaks to the proof adverse to the recommendation p. The relationship of a couple (μ ,λ) with a suggestion p implies that the level of ideal proof at p is μ , and the level of adverse proof at p is λ. As indicated by the comments in the related lattice appeared in figure-8(b)) [27]

- (1,1) → shows the presence of both, ideal and adverse proof totals, with a logical meaning of irregularity to the recommendation p.
- (1,0)→ shows the presence of complete ideal proof with adverse proof equal to zero, flagging an undertone of logical truth for the recommendation p.
- (0,0)→ shows the presence of ideal and adverse proof with the two values equal to zero, doling out a logical implication of uncertainty for the recommendation p.
- (0,1) → demonstrates the presence of ideal proof equal to zero and all out adverse proof, flagging a meaning of logical lie for the recommendation p.

The conditions of the PAL2v are acquired through a change where, at first, are viewed as characterised in a Unit Square in the Cartesian Plane (USCP) the level of ideal evidence μ in the y - axis, and the level of adverse evidence λ in the x - axis, as indicated by Figure-8(c)[26] - [28] A change that permits the degrees of proof of standardized qualities characterised in the x , y axis of the (USCP) to be situated on the X and Y axis of a four vertex PAL2v Lattice, given by equation - 36.

$$T(X, Y) = (xy, x + y - 1) \tag{36}$$

$$D_c = \mu - \lambda \tag{37}$$

$$D_{ct} = \mu + \lambda - 1 \tag{38}$$

$$\varepsilon\tau = (D_c D_{ct}) \tag{39}$$

$$\mu_{ctr} = (\mu + \lambda)/2 \tag{40}$$

$$d = \sqrt{(1 - |D_c|)^2 + (D_{ct})^2} \tag{41}$$

If $D_c > 0$

$$D_{CR} = 1 - \sqrt{(1 - |D_c|)^2 + (D_{ct})^2} \tag{42}$$

If $D_c < 0$

$$D_{CR} = \sqrt{(1 - |D_c|)^2 + (D_{ct})^2} - 1 \tag{43}$$

$$\mu_{ER} = (D_{CR} + 1)/2 \tag{44}$$

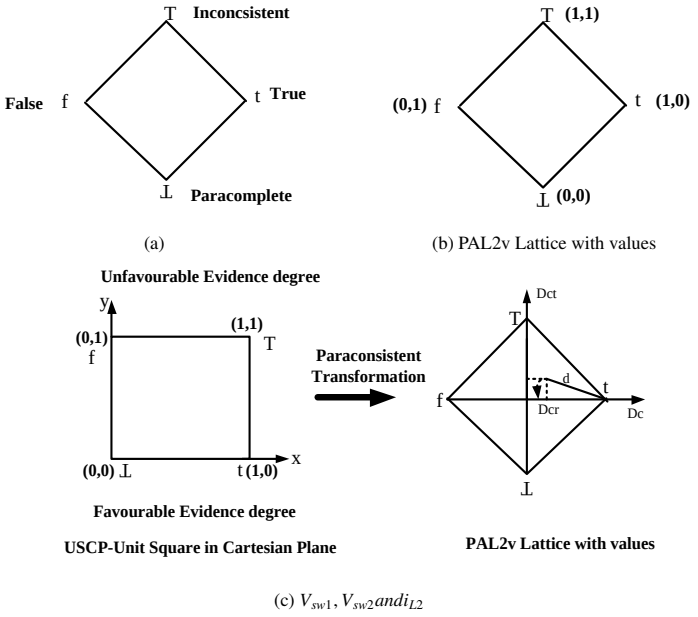


Figure 8: (a) Lattice associated with annotation of two values PAL2v. (b) PaL2v – Hasse finite Lattice with annotation. (c) Unit Square in the Cartesian Plane

Relating the parts of the change T(X , Y) concurring to the typical classification of PAL2v, where [26] - [28]: x = μ → Ideal Evidence degree, with $0 \leq \mu \leq 1$ and y = λ → level of Adverse Evidence, with $0 \leq \mu \leq 1$, where:

- The principal term acquired in the arranged match of the change condition is X = x-y = $\mu - \lambda$ → which will be known as the conviction degree D_c [27] - [29]. Accordingly, the conviction degree is acquired by equation - 37.
- The second term got in the arranged match of the change condition is: Y = x+y-1 = $\mu + \lambda$ - 1 → which will be known as the Contradiction Degree-Dct [27] - [29]. In this manner, the level of Contradiction is acquired by equation - 38.

The conditions of PAL2v permit the paraconsistent logical states to be found inside the lattice, the interpolation point is given by equation - 39. One can in this way settle on choices dependent on the vicinity of the logic state $\varepsilon\tau$ to the extraordinary logic states True (t) or False (f), found at the vertices of the PAL2v lattice. The Normalized Degree of Contradiction - μctr ,where a variety somewhere in the range of 0 and 1 is gotten, can be determined through condition [27] - [29] given in equation - 40. The Real Certainty degree D_{CR} is acquired by deciding the separation d in the PAL2v lattice as given in equation - 41. The (D_{CR}) values are determined by

the conditions appeared underneath [26] - [28] is given in equation - 42 and equation - 43 also linked by equation equation - 44.

The conditions gotten by the understandings made in the lattice related to PAL2v permit the making of algorithms utilized in examination and logical treatment of data signals. The Paraconsistent Analysis Node (PAN) algorithm can be utilized in a few fields of learning where fragmented and opposing data is dealt with fittingly through the PAL2v conditions. In this work, the PAN will be utilized to assemble a system of signals examination that embodies the control factors in a new converter.

4.3 Paraconsistent Algorithm

The explanation of a common PAN algorithm is specified under [26] - [28] State: P_1=input 1; P_2=input 2; O_1=outpu 1; O_2=output 2; O_3=output 3;

1 $\mu_1 = P_1$ (Ideal Evidence Degree), where $0 < \mu_1$. $\mu_2 = P_2$ (Ideal Evidence Degree), where $0 < \mu_2$.
$\lambda = 1 - \mu_2$ (Adverse Evidence Degree), where $0 < \lambda < 1$.

2 Evaluate the conviction degree $D_c = \mu 1 - \lambda$

3 Evaluate the degree of conviction $D_{ct} = \mu 1 + \lambda - 1$

4 Evaluate Normalized Degree of Contradiction. $\mu_{ctr} = (\mu 1 + \lambda)/2$

5 Evaluate the separation d in the PAL2v lattice. $d = \sqrt{(1 - |D_c|)^2 + (D_{ct})^2}$

6 Decide the output signals. If d > 1, then keep O_1=0.5; O_2= μ_{ctr} and $O_3 = D_{ct}$. Consider meaning less and go to exit. Else move to the next step

7 Decide actual conviction degree D_C. If $D_C > 0$ evaluate $D_{CR} = 1 - \sqrt{(1 - |D_c|)^2 + (D_{ct})^2}$
If $D_C < 0$ evaluate $D_{CR} = \sqrt{(1 - |D_c|)^2 + (D_{ct})^2} - 1$

8 Determine Resultant Real Evidence degree.
$\mu_{ER} = (D_{CR} + 1)/2$

9 The Real outputs are O_1=μ_{ER} , $O_2 = \mu_{ctr}$ and O_3= D_{ct} .

10 End.
In this article the Evidence degree was created as follows:
$0<\mu_2<1$ are proportional to $0.2V<P_2<14V$ and
$0<\mu_1<1$ are proportional to $0V<P_1<14V$.
$14V \rightarrow \mu_1 = 1$; with For $P_1 = 0V \rightarrow \mu_1 = 0$; and $P_1 = arelationof \mu_1 = P_1/14$.
$14V \rightarrow \mu_2 = 1$; with For $P_2 = 2V \rightarrow \mu_2 = 0$; and $P_2 = arelationof \mu_2 = (P_1 - 0.2)/14 and \lambda = 1 - \mu_2$.

5 Comparisons of Different Converters and the Control Technique

Table-I shows the comparisons of complexity, voltage gain, voltage and current stress, components of different converters such as traditional [30], Shan and Faqiang [20] and projected TA converter. Figure-9 curve shows the variation of voltage gain with the duty cycle. From observation it is clearly visible that TA converter provides a positive average inductor current but average inductor current under buck mode in Shan and Faqiang converter is negative. The peak inductor voltage V_{L2peak} and peak capacitor current I_{Cpeak} is less in TA converter. Figure-7 shows the comparison results of output voltage, inductor currents, switch voltages and source current between conventional PI and Paraconsistent logic based PI. From the figure it is clearly visible that the dynamic response of output voltage, inductor currents are faster in PL-PI than PI. It is also observed that for the same P and I gain the output voltage in PL-PI is obtained with less value of filter capacitor. The steady state values and time are same in both the controllers.

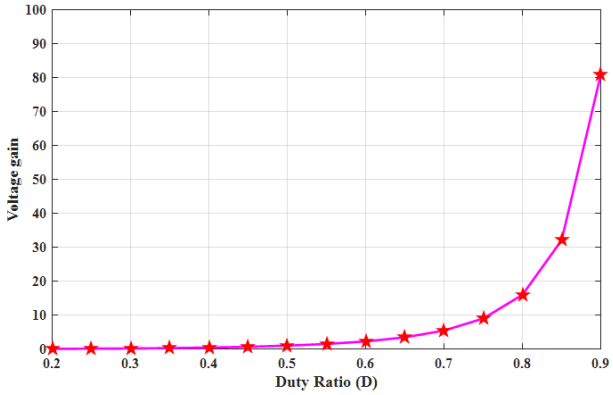


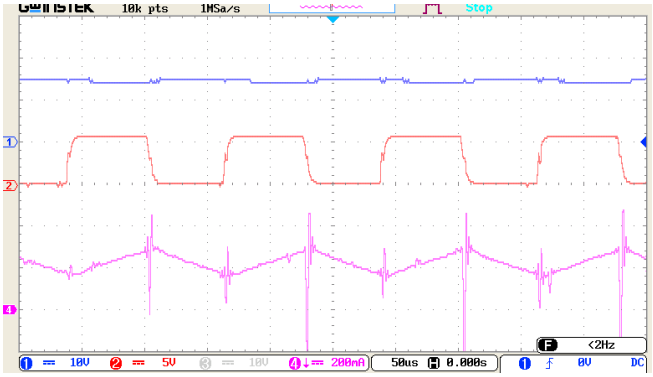
Figure 9: Voltage gain curve with duty ratio.

6 Hardware Parameters and Results

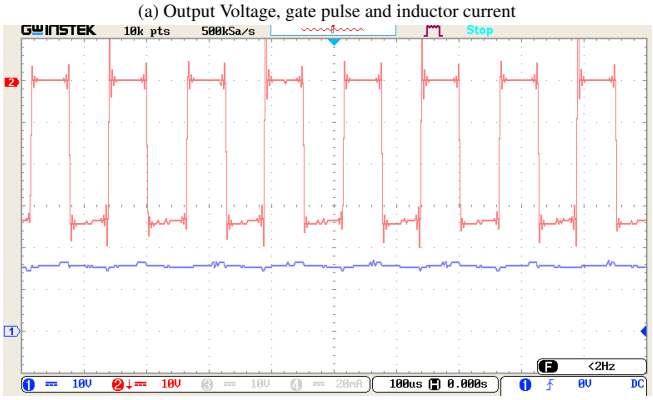
The parameters chosen for hardware implementation are provided in Table-II. PLPI controller is implemented for obtaining a fixed output voltage. The DSP (F28379D) Board is used for the designing of the proposed PLPI and traditional PI controller. The program is written in code composer studio and also the output file is burned on the DSP board using the same. Primarily a resistive load is taken to test the controller then the battery of rating 12volt 7Ah (Lead acid type) is taken as load. 1.4Amp of peak charging current is drawn by the battery. Figure-11 and Figure-10 shows the results in boost and buck mode respectively. Figure-12shows the photo of the complete hardware set up. Figure-13 which shows the efficiency curve explains clearly that efficiency in boost mode is higher than buck mode. The different results for battery load is shown in Figure-14.

7 Conclusion

A positive output based transformer less buck–boost (TA) converter is projected in this article. This converter overcomes several draw backs of the old-fashioned and Shan and Faqiang converter. The steady state operation principle, mathematical model, and performance comparisons with other converters are enlightened. The analysis is done using Matlab simulation and the verification of the same through experiment is done. This projected converter retains several merits in both boost and buck mode. This converter provides



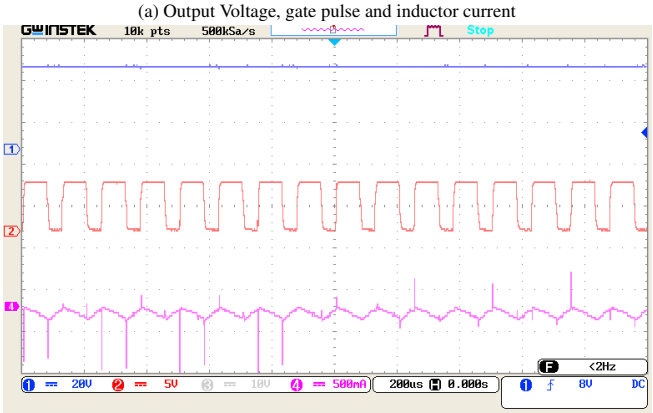
(a) Output Voltage, gate pulse and inductor current



(b) Capacitor and Diode Voltage

Figure 10: Buck mode results.

(a) Output Voltage, gate pulse and inductor current



(b) Capacitor and Diode Voltage

Figure 11: Boost mode results.

Figure 12: Picture of the hardware setup of the proposed TA Converter with DSP and PC interface.

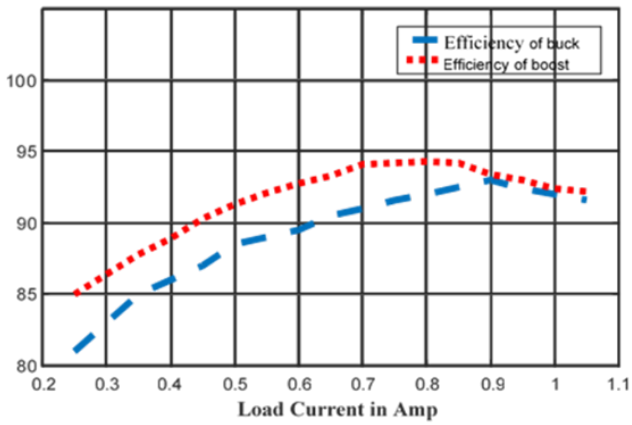


Figure 13: Efficiency Versus Load current for both Buck and Boost mode.

Figure 14: Output Voltage, gate pulse and inductor current for a Battery Load.

positive current through inductor and also provides positive output voltage. The converter control strategy is easy to implement. So, the planned converter is suitable for EV battery charging and industrial applications where high voltage gain is required. This article has also projected paraconsistent logic based PI controller. A comparison result is also shown in the figures. From the simulation and hardware result it is proved that the new control technique provides a better dynamic performance as well as provides better result with low value of capacitors.

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Table 1: Comparison of different buck-boost converters

Parameters	Conventional Buck-Boost Converter [30]	Shan and Faqiang Converter [20]	TA converter [19]
Switches	1	2	2
Diodes	1	2	2
Capacitors	1	2	2
Inductors	1	2	2
Voltage gain	$\frac{D}{(1-D)}$	$(\frac{D}{(1-D)})^2$	$(\frac{D}{(1-D)})^2$
(Voltage stress on Switch-1)/V_S	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$
(Voltage stress on Switch-2)/V_S		$(\frac{D}{(1-D)})^2$	$(\frac{D}{(1-D)})^2$
Nature of average Inductor current	Positive	Negative	Positive
complexity	2^{nd} order	4^{th} order	4^{th} order
Peak Voltage of L_2	V_C	V_{C1}+V_{C2}	V_{C2} or V_{C1}
Peak current through C_1	I_{Lmax}	I_{L1max} + I_{L2max}	I_{L1max} or I_{2Lmax}

Table 2: Different parameters of TA [19] converter

Parameters	Values	Parameters	Values	Parameters	Values
Inductor L_1	1 mH	V_S	18 Volt	Diodes	1N
Inductor L_2	3.5 mH	Proportional gain	0.0145	Load Resistance for Buck	5-50ω
Capacitor C_1	1μF (PL-PI) and 100μF (PI)	Integral gain	39.346	Load resistance for Boost	40 - 160 ω
Capacitor C_2	1μF (PL-PI) and 220-1000μF (PI)	Switches	MOFET IRF	Battery	Lead Acid 12V, 7AH